Session C9

Nyquist ADC

Wednesday, June 20, 10:05 a.m.

HONOLULU SUITE

Co-Chairs: R. Kapusta, Analog Devices
C. Liu, MediaTek, Inc.

C9-1 - 10:05 a.m.
A 12-bit 31.1uW 1MS/s SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4dB SFDR using 256fF Sampling Capacitance, J. Shen, A. Shikata, A. Liu, F. Chalifoux, Analog Devices

C9-2 - 10:30 a.m.
A 0.5-1.1V 10b Adaptive Bypassing SAR ADC Utilizing Oscillation Cycle Information of VCO-based Comparator, Z. Ding, X. Zhou, Q. Li, University of Electronic Science and Technology of China

C9-3 - 10:55 a.m.
A 2.3-mW, 950-MHz, 8-bit Fully-Time-Based Subranging ADC Using Highly-Linear Dynamic VTC, K. Ohhata, Kagoshima University

C9-4 - 11:20 a.m.

C9-5 - 11:45 a.m.