Session C16

Hardware Security

Thursday, June 21, 8:10 a.m.
TAPA 1

Co-Chairs: B. Calhoun, University of Virginia
N. Miura, Kobe University

C16-1 - 8:10 a.m.

C16-2 - 8:35 a.m.

C16-3 - 9:00 a.m.
An All-Digital True-Random-Number Generator with Integrated De-correlation and Bias-Correction at 3.2-to-86 Mb/s, 2.58 pJ/bit in 65 nm CMOS, V. Pamula, X. Sun, S. Kim, F. Rahman, B. Zhang and V. Sathe, University of Washington

C16-4 - 9:25 a.m.
220mV-900mV 794/584/754 Gbps/W Reconfigurable GF(2^4)^2 AES/SMS4/Camellia Symmetric-Key Cipher Accelerator in 14nm Tri-gate CMOS, S. Satpathy, V. Suresh, S. Mathew, M. Anders, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, Intel Corporation