A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit

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Abstract

This paper presents a fully integrated digital low-dropout regulator (LDO). A proposed event-driven digital control based on a residue-tracking loop provides not only a heavy load capacity of 700mA but also an accurate regulation. A latch-based shift register is adopted to improve the digital regulation against a large load current change. The proposed LDO embedding an on-chip 100pF output capacitor was fabricated in a 65nm LP CMOS process. The LDO provides a load regulation of 0.1mV/mA and an output voltage error below 1.1% across a range from 0.5 to 1V. The LDO achieves a figure-of-merit (FOM) of 6.744.

Introduction

Recently developed system-on-chips (SoCs) integrate a number of analog/digital blocks that have a large power consumption. To provide optimized power supplies to the various blocks depending on a system operation, the SoCs adopt a dynamic voltage scaling (DVS) technique. Hence, a fine-grained power management unit (PMU) with multiple low-dropout regulators (LDO) is introduced for the SoCs [1-5] as shown in Fig. 1. Although line regulation burden of the LDO can be relaxed owing to a power-efficient switching regulator, the fine-grained PMU imposes several challenging requirements on the LDO: a) a heavy load capacity up to hundreds of milliamperes with a fast transient response, b) a fully integrated structure without an external capacitor, and c) an accurate regulation with a wide output range for the DVS technique. In case of a clock-based time-driven digital LDO [1-3], a high-frequency clock is required to reduce voltage droop by a sudden load change, resulting in significant power consumption to be distributed over the SoCs. An event-driven LDO [4] and an asynchronous LDO [5] were proposed, but they have problems of small load capacity and low accuracy.

In this paper, we present a fully integrated event-driven digital LDO with a residue-tracking loop (RTL). The event-driven operation with assistance of the RTL enables the digital controller to handle heavy load change of 700mA rapidly without any clocking source. The digital controller employs a latch-based shift register that provides faster load regulation than a conventional clock-based shift register.

Architecture and Implementation

Fig. 2 illustrates the conceptual diagram of the proposed regulation scheme. To eliminate the clock distribution burden and sampling clock dependency of the output voltage droop, the proposed LDO adopts the event-driven operation triggered by a load current variation. The RTL senses the load current variation using a residue current. Assuming that the load current is $I_{LOAD}$ and the digital LDO output current is $I_{DLDO}$, the residue current $I_R$ is a difference between $I_{LOAD}$ and $I_{DLDO}$, corresponding to a current quantization error of the digital regulation. Hence, the RTL tracks $I_R$ which satisfies $I_{LOAD} - I_{DLDO} = I_R$ ($0 \leq I_R \leq I_{R,MAX}$). When $I_{LOAD}$ becomes larger than $I_{DLDO} + I_{R,MAX}$ (i.e., $I_R \geq I_{R,MAX}$), the digital controller increases the number of turn-on digital pass gates, $N$, in order to find $I_{DLDO}$ that satisfies $I_{DLDO} < I_{LOAD} \leq I_{DLDO} + I_{R,MAX}$. On the other hand, when $I_{LOAD}$ becomes smaller than $I_{DLDO}$ (i.e., $I_R = 0$), the digital controller reduces $N$ until $I_{DLDO}$ is not larger than $I_{LOAD}$. Otherwise, the digital controller maintains $I_{DLDO}$ as a freeze status. In this manner, the RTL senses the load current variation and triggers the event-driven operation of the digital controller. It is noteworthy that the RTL tracks $I_R$ by sensing the control voltage $V_{CTRL}$. Compared to the sensing of the LDO output voltage $V_{OUT}$ [4], the proposed RTL achieves a uniform residue-current sensing regardless of the digital LDO output current. The RTL also provides a fine voltage regulation during the freeze status of the digital controller.

Fig. 3 shows the block diagram of the proposed LDO which is composed of a residue-driven trigger, a digital controller, a bidirectional latch-based shift register, a digital pass gate array, and an on-chip 100pF output capacitor. The residue-driven trigger is implemented with the RTL and continuous-time residue detector. To achieve a stable regulation with the on-chip 100pF output capacitor along with a wide output voltage range, the RTL employs a rail-to-rail high slew-rate OTA with a cascode-compensation technique. The width of pass gate in the RTL is designed as three times of the digital pass gate to reduce a voltage ripple during the digital regulation. The residue detector is implemented with continuous-time comparators that sense $V_{CTRL}$ in the RTL. When the $V_{CTRL}$ becomes lower than $V_T$ or higher than $V_T$, the residue detector forces the digital controller to start the digital regulation by enabling transitions in the bidirectional latch-based shift register.

Fig. 4 shows the detailed schematics of the digital loop controller and the latch-based shift register. The digital loop controller is implemented with a transition controller and an up/down controller. The transition controller enables or disables the transition in the shift register according to the residue detector output. The up/down controller determines shifting direction: forward or backward direction that corresponds to incrementing or decrementing $N$, respectively. To support a fast regulation against a sudden load current change, the proposed LDO adopts the latch-based shift register. Owing to an asynchronous propagation between the latch stages, the latch-based shift register can track the load current variation faster than that of the flip-flop-based shift register [1-3]. The shift register is composed of 64 latch stages. Each latch stage includes a multiplexer, an inverter-based latch, a digitally-controlled delay line (DCDL), and a pre-driver. The multiplexer selects pre- or post-bit data based on the direction of the up/down controller. Then, the inverter-based latch updates the selected data. To prevent a limit cycle oscillation during the digital regulation, the DCDL is employed to adjust the propagation delay between the latch stages. Each control data in the latch stages is applied to corresponding digital pass gates through the pre-drivers.

Experimental Results

The proposed LDO was fabricated in a 65nm LP CMOS process. It supports a load capacity of 700mA with a quiescent current of 254μA. The output voltage range of the LDO is from 0.5 to 1V for a 1.2V input voltage. Fig. 5 shows the measured transient response of the proposed LDO. When the on-chip test block draws the step load current from 0 to 700mA with the edge time of 100ns, the measured voltage droop caused by the step load increase is 130mV. Fig. 6 shows the measured output voltages of the LDO depending on the load current. The LDO maintains output voltage of 1V across the load current range from 0 to 700mA, providing the load regulation of 0.1mV/μA. Fig. 7 shows the measured output voltage errors of five fabricated LDO samples within $V_{REF}$ range from 0.5 to 1V. Owing to the fine regulation by the residue-tracking loop, the proposed LDO keeps
the voltage error within 1.1% across the range of $V_{REF}$. Table I summarizes the measurement results of the fabricated LDO. The proposed LDO achieves the lowest FOM of 6.74s compared with the prior works [1-5]. The comparison of FOM with recent works on the LDO is illustrated in Fig. 8. A die microphotograph of the fabricated LDO is also shown in Fig. 8. The active area of the LDO is 0.113mm² including the on-chip 100pF output capacitor.

References