An Ultra-low Quiescent Current 250nA Low Dropout Regulator for No-load to 10mA

Internet-of-Everything Applications

Shao-Qi Chen\textsuperscript{1}, Chia-Ming Huang\textsuperscript{1}, Ke-Hong Chen\textsuperscript{1}, Ying-Hsi Lin\textsuperscript{1}, Shian-Ru Lin\textsuperscript{1}, Tsung-Yen Tsai\textsuperscript{2}

\textsuperscript{1}National Chiao Tung University, \textsuperscript{2}Realtek Semiconductor Corp, Hsinchu, Taiwan

Abstract

The proposed analog low-dropout regulator (ALDO) achieves 250nA of ultra-low quiescent current and 130μA of fast transient response simultaneously. The proposed use of an ultralow quiescent current (ULQC) error amplifier to regulate the gate of power MOSFET while the auxiliary digital gate voltage control (DGVC) circuit contributes to the load transient response. Moreover, the switching frequency is dynamically reduced by the frequency modulation after entering the steady state. The line and load regulation rates are 0.14mV/V and 0.21mV/mA, respectively. High current efficiency of 99.91% and the best merit-of-figure in steady state are achieved.

I. Introduction

For Internet-of-Everything (IoE), portable and wearable devices, an ultra-low quiescent current LDO regulator is essential as it can effectively extend battery lifetime. The three-loop capacitorless ultra-low quiescent current LDO regulator is needed to regulate the power dissipation. Fig. 3 shows the proposed ALDO with the DGVC technique. The proposed ALDO in Fig. 2 regulates V\textsubscript{OUT} through an analog loop with an ultralow I\textsubscript{q} and fast transient response. ULQC EA ensures load regulation accuracy. Thus, this paper proposes an ALDO to achieve both features to meet the requirements.

II. Proposed ALDO with the DGVC Technique

For Internet-of-Everything (IoE), portable and wearable devices, an ultra-low quiescent current LDO regulator is essential as it can effectively extend battery lifetime. The three-loop capacitorless ultra-low quiescent current LDO regulator is needed to regulate the power dissipation. Fig. 3 shows the proposed ALDO with the DGVC technique. The proposed ALDO in Fig. 2 regulates V\textsubscript{OUT} through an analog loop with an ultralow I\textsubscript{q} and a transient response of less than 1μs at a full load step of 10mA. The auxiliary DGVC circuit. The DGVC quickly adjusts the V\textsubscript{OUT} while entered by the ultralow quiescent current EA if there is any load change. Therefore, V\textsubscript{OUT} is regulated using a proposed fast response digital gate voltage control (DGVC) circuit.

The proposed ALDO regulator in Fig. 2 regulates V\textsubscript{OUT} through an analog loop with an ultralow I\textsubscript{q} of less than 250nA and a transient response of less than 1μs at a full load step of 10mA by the auxiliary DGVC circuit. The DGVC quickly adjusts V\textsubscript{OUT} for fast transient response. At the same time, ULQC EA loses control of the V\textsubscript{OUT} as a weak driving source. Therefore, V\textsubscript{OUT} is restored to its nominal value, the DGVC shuts down again and hands over control to the ULQC EA for ultralow I\textsubscript{q} operation. Simultaneously, ULQC EA and DGVC circuits achieve ultra-low I\textsubscript{q} and fast transient response, respectively.

III. Circuit Implementations

A. ULQC EA and the Q factor suppression (LLQS) technique

The proposed analog low-dropout regulator (ALDO) achieves 250nA of ultra-low quiescent current and 130μA of fast transient response simultaneously. The proposed use of an ultralow quiescent current (ULQC) error amplifier to regulate the gate of power MOSFET while the auxiliary digital gate voltage control (DGVC) circuit contributes to the load transient response. Moreover, the switching frequency is dynamically reduced by the frequency modulation after entering the steady state. The line and load regulation rates are 0.14mV/V and 0.21mV/mA, respectively. High current efficiency of 99.91% and the best merit-of-figure in steady state are achieved.

B. DGVC circuit

For Internet-of-Everything (IoE), portable and wearable devices, an ultra-low quiescent current LDO regulator is essential as it can effectively extend battery lifetime. The three-loop capacitorless ultra-low quiescent current LDO regulator is needed to regulate the power dissipation. Fig. 3 shows the proposed ALDO with the DGVC technique. The proposed ALDO in Fig. 2 regulates V\textsubscript{OUT} through an analog loop with an ultralow I\textsubscript{q} and fast transient response. ULQC EA ensures load regulation accuracy. Thus, this paper proposes an ALDO to achieve both features to meet the requirements.

The paper presents an ALDO to achieve both features to meet the requirements.

Experimental Results

Fig. 8 shows the measurement results during a transient response with a load change of 10 mA. When the DGVC control is disabled, undershoot and overshoot are 450mV and 150mV, respectively. A large load step of 10mA achieves the best Figure-of-Merit 1 (FOM) of 0.135%. FOM: including transient response T\textsubscript{e} is worse than [1], but large I\textsubscript{q} is consumed in [1]. Chip micrograph is shown in Fig. 10.

References

Fig. 1. (a) Leakage at the gate of power P-MOSFET. (b) Leakage rate of VG in different operation regions.

Fig. 2. The proposed LDO concept with an assisted DGVC loop to achieve both ultralow quiescent current and fast transient response.

Fig. 3. Proposed ULQC LDO with Light Load Q Factor Suppression (LLQS) technology.

Fig. 4. Small signal analysis, Q-factor expression, and frequency response.

Fig. 5. Circuit implementation of the DGVC circuit.

Fig. 6. Timing diagram of the DGVC operation.

Fig. 7. DGVC stability analysis.

Fig. 8. Measured transient response when I_{load} changes from 0 to 10mA and vice versa, including zoom-in undershoot, overshoot and recovery time without the DGVC in (a) and with the DGVC in (b). (V_{in}=1.1V, V_{REF}=0.5V, V_{OUT}=1.0V, I_{LOAD}=0~10mA, C_{G}=10pF, and F_{CLK}=20MHz)

Fig. 9. Performance statistics.

Fig. 10. Measured statistics and chip micrograph.

Table I: Specifications and comparison table with state-of-the-arts.