A 95.3% Peak Efficiency, 135nA Quiescent Current Buck-Boost DC-DC Converter
with Current-Slope-Based Mode Control
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Abstract
A current-slope-based mode control method is proposed for a buck-boost DC-DC converter to realize automatic mode switching between buck and boost in one switching period without additional quiescent current (IQ). Implemented in 0.18μm CMOS, the converter realizes 95.3% peak efficiency and above 90% over a load range from 15μA to 200mA. Accurate current slope measurement is achieved with initial sampling and 135nA total IQ is achieved with a zero-IQ pull-up structure in the input monitor.

Introduction
Vital sign monitoring (VSM) functions such as Heart rate (HR) and oxygen saturation (SPO2) are common in wearable devices for health and fitness tracking. As shown in the system architecture in Fig. 1, a noninverting buck–boost converter should be employed to power diverse types of LEDs over the entire battery voltage range. In optical measurement system, a pulsed current with 0.13% to 2% duty cycle is used to drive the LED, giving an average current that could be as low as 23μA [1]. As such, the power consumption of the regulator in standby mode determines the total battery lifetime. Therefore, an ultra-low quiescent current (IQ) buck-boost converter is demanded to achieve high efficiency at tens of μA average load current and thus extends battery longevity. However, the efficiency of buck-boost converters reported to date cannot reach 90% for load currents less than 10mA, due to the large IQ of automatic mode detection which is used to improve the efficiency of the conventional buck-boost control scheme [2-5]. Although hysteretic-current-mode control with discontinuous conduction mode [3] tries to enhance the efficiency in light load, the associated power dissipation of the error amplifier and current monitor still limits its efficiency for sub-mA loads.

In this paper, a current-slope-based mode (CSBM) control method is proposed to realize fast automatic mode transition between buck and boost without any additional IQ.

Architecture and Principles of Operation
Fig. 1 illustrates the block diagram of the buck-boost converter with CSBM control. When VOUT falls below the reference voltage, all blocks are enabled to charge the output capacitor. The inductor current (IL) ramps between peak current limit (Ith_peak) and zero until VOUT exceeds the hysteresis window and the converter goes into sleep phase. To save IQ, only the voltage & current reference, hysteresis comparator and zero IQ input monitor are kept alive, which are essential for valid output regulation.

The operating principle of CSBM control is described by the state transition graph in Fig. 2. Φ1 is the sleep phase with all switches off. In buck mode when hysteresis comparator output (CMP) becomes high, the converter goes to Φ3 until IL increases to Ith_peak and then to Φ4 until IL decreases to zero. Since the rising slope of IL is proportional to VIN-VOUT, if IL is lower than Ith_min at T1 delay after S1 is turned on, it means VIN is close to VOUT so the mode changes to boost. An overtime (OT) check is applied at T2 delay after S1 is turned on as a failsafe mode detection, in case VIN changes between T1 and T2. If S1 is still on at T2, the converter transitions into boost mode. While in boost mode, the converter switches between Φ2 and Φ5 according to the IL with the same limit thresholds. Since the falling slope of IL is proportional to VIN-VOUT, if IL is larger than Ith_max at T1 delay after S4 is turned on, the mode changes back to buck. The OT check is also applied at T3 delay after S4 is turned on to avoid any dead zones in mode detection. When the CMP signal goes low, the converter returns to sleep phase Φ1. Since Ith_peak is much larger than the load current, VOUT is quickly charged up if the IL slope is near zero and the converter switches to sleep phase automatically. Therefore, no efficiency deterioration appears when VIN approaches VOUT since conventional buck-boost mode [4,5] is not applied.

With CSBM control, the mode transition is completed in one switching period as illustrated in Fig. 3. Considering a voltage falling at VIN, at the first switching cycle IL is lower than Ith_min at the check point, thus the mode is changed to boost immediately and IL ramps up with S3 turned on. After IL reaches Ith_peak, S4 turns on to charge the output capacitor. The next switching cycle does not start until IL crosses zero. For the case of VIN rising, IL reaches Imax before the Imax check point when S1 and S4 turn on at the first switching cycle, so the converter is set to buck mode. Therefore, the mode transition is completed in one IL switching cycle with CSBM control. Since it is only enabled during switching phase, the additional IQ for mode detection in sleep phase [3] is eliminated.

Circuit Implementations
An exact IL slope measurement is necessary for CSBM control, but the delay and blank time of a conventional current comparator would deteriorate the accuracy if a fixed current threshold were used for both Ith_min and Ith_max. Therefore, an IL slope comparator with initial IL sampling is proposed to solve this issue as shown in Fig. 4(a). C0 is used to sense the initial value of IL at ΦA when the blank signal of the comparator is high. Then the IL initial value is subtracted by a four-input comparator at ΦB to get the accurate slope value. Since the IL slope comparison is realized by delay comparison between Tc and Imax check delay T1 (Fig. 2), it can be simply implemented through logic cells.

To further reduce IQ, the zero IQ input voltage monitor, which can disable or reset the chip if the input voltage is lower than minimum operation supply voltage without power consumption, is proposed as Fig. 4(b). A zero IQ pull-up structure composed by a native NMOS (Mnt) and a medium Vth PMOS (Mpm) pulls up Vp to VIN when VIN is just larger than Vth of Mpm. After Vdd rises, the current of the pull-down path (Mn1 and Mn2) increases, pulling Vp low. Meanwhile, Mnt and Mpm are both turned off as [Vth] increases due to body effect, so zero IQ is realized for negligible pull-up current in normal operation.
**Experimental Results**

The ultra-low IQ buck-boost converter is fabricated in a 0.18μm CMOS process. Wide output voltage range (1.8V-5.5V) and input voltage (2.3V-5.5V) are achieved with 200 mA maximum load current (600mA peak IL). Fig. 5 shows the measured steady-state waveforms when Vout=3.3V with 200mA peak IL for different input voltages. When the voltage difference between VIN and VOUT is small, the switch S1 and S4 are almost always ON during the switching phase until the difference between VIN and VOUT is larger than rising threshold. The line transient responses are shown in Fig. 6 with 25mV/VOUT rising/falling speed. The mode transition is completed at the rising/falling speed. The mode transition is completed at the first switching cycle after VIN exceeds the threshold. 135nA rising/falling speed. The mode transition is completed at the falling rise of VIN.

The measured steady-state waveforms when Vout=3.3V with 200mA peak IL and input voltage (2.3V–5.5V) are achieved with micrograph is depicted in Fig. 9 with a total area of 1mm2.

The measured peak efficiency reaches 95.3% when both VIN and VOUT are 3.6V and 20mA load, and over 90% efficiency is achieved for above 15μA load as shown in Fig. 8. The complete performance comparison to the state-of-the-art buck-boost converters is shown in Table I. The chip micrograph is depicted in Fig. 9 with a total area of 1mm2.

**References**