A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency

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Abstract
This paper presents a sub-harmonic switching (SHS) digital power amplifier (PA) architecture that enhances power efficiency in the power back-off (PBO) region. The proposed technique is combined with Class-G operation and, using either SHS or dual-power-supply switching, can provide more peak efficiency points, located at 0, -3.5, -9.5 and -13dB PBO. Moreover, by judiciously choosing the optimal operation mode (between SHS and dual supplies) for each PA cell at different power output levels, we can further improve the efficiency between those peaks. The SHS PA prototype is implemented with a switched capacitor PA (SCPA) architecture in 65nm CMOS. It achieves a 26.8dBm peak output power with a 49.3% peak drain efficiency (DE) and a 27% -13dB PBO DE at carrier frequency of 2.25GHz.

Keywords: sub-harmonic, Class-G, CMOS PA, power back-off, power amplifier, efficiency, SCPA, polar transmitter.

Introduction
With the trend of increasing data throughput, modern wireless communications prefer high-spectral-efficiency modulations, often leading to high peak-to-average-power ratios (PAPRs) for transmitted signals. Consequently, power amplifiers (PAs) need to operate in the PBO region most of the time. Conventionally, PAs yield the highest efficiency at the peak power. However, efficiency dramatically degrades as the PA output power scales back. Therefore, addressing the PA PBO efficiency is critical for achieving a high average power efficiency. Existing PA efficiency enhancement techniques in the PBO region, such as Doherty and outphasing PA, require relatively complex input preconditioning and extra power combiners at the output. Envelope-tracking PAs provide good average efficiency but suffer bandwidth limitations and require linear supply modulators. To alleviate those issues, we propose SHS technique to improve PBO efficiency with relaxed input preconditioning and without sophisticated supply modulators or power combiners at the PA output.

Proposed DPA Architecture and Implementation
Fig. 1 shows how proposed SHS PAs compare with conventional SCPAs [1]. Conventional SCPAs achieve 100% efficiency at the peak output power, assuming ideal PA drivers. At the peak output power, all amplifiers are toggled around the RF carrier frequency ($f_c$), which is the fundamental switching frequency. When the PA operates in the PBO region, the power efficiency starts to roll off due to a charge loss through the capacitor array. For example, Fig. 1a shows that two thirds of the capacitors are connected to ground to achieve a power back-off of 9.5 dB via a capacitor divider, and hence the charge loss. The key principle of the proposed SHS is to toggle PA cells at a sub-harmonic frequency ($f_0/3$ in Fig. 1b) while the PA output matching network selects its third harmonic component, i.e. the desired RF carrier frequency ($f_0$). Since the third harmonic component naturally possesses less power (-9.5 dB, in this case), it achieves the PBO without using the capacitor divider, avoiding the charge loss and, hence, creating a peak efficiency point in the PBO region. Another advantage of toggling at a slower sub-harmonic rate is the reduced power consumption by other front-end circuitry such as polar combiners, which increases the overall transmitter efficiency. Notably, the SHS technique can utilize any sub-harmonic component to create multiple efficiency peaks, if desired.

Moreover, the proposed SHS can be combined with Class-G operation to achieve more efficiency peaks in the PBO region (Fig. 2). Toggling the entire PA cells at either sub-harmonic or lower power supply creates four efficiency peaks. Between the peaks, we use a hybrid switching scheme that combines SHS and dual-supply Class-G operation, such that the power efficiency is enhanced at all output power levels. The switching scheme of a simplified version (a 4-bit capacitor array) is shown in Fig. 3; the actual implementation is 8-bit.

The proposed PA implementation contains AM and PM paths (Fig. 4) for polar modulation. A phase generator first creates the delayed PM signal and the sub-harmonic PM signal via a divide-by-3 block for SHS operation. The synthesized decoder converts the 8-bit amplitude code into three signals: phase control, amplitude and supply control. The phase control signal is synchronized with the PM signal to create a glitch-free MUX control signal. The high-speed MUX selects the desired toggling frequency for each PA cell based on the hybrid switching scheme. To further improve the efficiency of the unit PA cell, a non-overlapping clock is used to minimize the crowbar current.

Fig. 5 shows the PA unit cell, including the output drivers and pre-drivers. Depending on the supply control signal, the output driver operates on either a 3.6V or 2.4V power supply. Three-stacked devices are used to achieve a high output power. To minimize the voltage stress, deep n-well (DNW) transistors are used in the driver. The DNW layer connects to 3.6V through a large resistor to avoid forward-biased diodes and minimize parasitic loss. The simulated load-pull contours show the optimal impedance for deriving the peak efficiency and maximum output power of this design.

Measurement Results
The measured power efficiency improves as much as 2.6X at -13dB PBO over Class-B via the proposed SHS with hybrid Class-G operation (Fig. 6); Fig. 7 shows the die photo. Fig. 8 shows the AM-AM and AM-PM responses used for digital pre-distortion and the PA efficiency and output power versus frequencies. The PA delivers a 26.8dBm peak power with a 49.3% DE with a -3dB bandwidth of 500MHz. Fig. 9 shows the dynamic performance of the PA using a 5-MHz 16-QAM OFDM signal (7.2dB PAPR). It achieves an 18.5dBm average power and a 35.7% average DE with a -26dB EVM and a -34dBc ACRP, using real-time SHS with hybrid Class-G operation (Fig. 3). Lastly, Table I shows that the proposed PA achieves a superior PBO efficiency compared to state-of-the-art CMOS PAs using other PBO efficiency enhancement techniques.
Fig. 1. Conventional SCPA versus proposed SHS PA in PBO

Fig. 2. Proposed SHS with hybrid Class-G operation

Fig. 3. Simplified PBO operation table

Table I. Comparison with other PBO efficiency-enhanced CMOS Digital PAs

References


Fig. 4. Block diagram of the proposed PA implementation

Fig. 5. Proposed PA unit cell (active part)

Fig. 6. Measured P_out versus DE at 2.25 GHz

Fig. 7. Chip microphotograph

Fig. 8. Measured CW performance

Fig. 9. Measured EVM and spectrum using modulated signals