A 1.2V 68μW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator
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Abstract
This paper presents a micro-power audio continuous-time delta-sigma modulator. Fabricated in a 65nm CMOS process, the modulator occupies 0.14mm² and achieves 98.2dB DR, 94.1dB SNDR and 107dB SFDR in a 24kHz BW while consuming only 68μW from a 1.2V supply. This results in a Schreier FoM of 183.6 dB, the highest energy-efficiency for audio ADCs published to date.

Introduction
Design of a low-power continuous-time delta-sigma modulator (CTDSM) without performance degradation is a challenging task [1]-[4]. Several techniques, such as assisted opamp [2], feedback FIR DAC [3], multibit alternative [4], have been investigated to mitigate the performance degradation, but they often result in design complexity. A negative-R assisted integrator technique in [1] relaxes the opamp’s requirements and results in micro-power consumption, but the SNDR is limited to 85.5dB. This paper describes a highly linear audio CTDSM that achieves 98.2dB DR, 94.1dB SNDR and 107dB SFDR in a 24kHz BW while consuming only 68μW, resulting in a Schreier FoM of 183.6dB. These advances are achieved by the combination of an optimized loop filter, a negative-R assisted integrator and a tri-level RDAC.

Proposed CTDSM
Fig.1 shows the architecture of the proposed CTDSM, the 3rd order CIFF structure with 1.5-b quantizer and tri-level feedback DACs. The modulator has a sampling rate of F_s=6.144MHz with OSR=128 and H_eq=1.7. The R_IN of 50kΩ is chosen to achieve a target DR (>98dB). Each integrator is implemented with an active-RC integrator assisted with a corresponding negative-R at the virtual ground. A passive adder with a signal swing of 600mV is realized at the input of the 1.5b quantizer. The 1.5b quantizer provides a well-defined quantizer gain of 1.6 and an improved stability over 1b CTDSM [1]. The excess-loop-delay (ELD) is compensated by direct feedback path around quantizer with passive adder and its pole location is set to be 15F_s. In contrast to [1], feedback DACs employ a resistive tri-level NRZ DAC, which mitigates the noise of clock jitter and the linearity requirement of the 1st integrator. Considering a clock jitter with 20ps RMS, the tri-level DAC exhibits an in-band noise of 94pV/√Hz, which is below the thermal noise level, where the clock jitter noise is about 4 times lower than that of the single-bit design.

A simplified schematic of the 1st integrator is shown in Fig.2(a). With the negative-R (-2(R_IN/R_DAC)) at the virtual ground, the input-referred noise of the 1st opamp including thermal noise and 1/f noise is shaped with a transfer function of sR_IN/C_IN, which attenuates an in-band noise without modifying the STF. Therefore, the 1st opamp can be implemented with a small g_m (=64μS) and short channel devices (<1μm). Since the noise of the 1st opamp is highly attenuated, the total thermal noise of the proposed CTDSM is estimated to be 20kT/C.IN.

Typically, the linearity of the 1st integrator is proportional to G_IN/R_IN. Since the R_IN is chosen to match the thermal noise level, the G_IN of the 1st opamp should be increased to maintain the linearity. However, as shown in Fig.2(b), the distortion current I_diss of the negative-R assisted integrator can be compensated directly at the virtual ground V_s, the HD3 of the integrator is reduced without increasing the G_IN of the 1st opamp. As a result, considering ±20% mismatch between the R_s and negative-R, the integrator represents more than 25dB improvement in HD3.

A detail configuration of the tri-level RDAC is described in Fig.3. A feedback symbol “0” is realized with a short circuit path by closing the M_s/M_b switches without using extra reference or DAC element. This guarantees the DAC linearity even if R_DAC mismatch and offset exist. Since the feedback symbol always pass through “0” i.e. from ±1 to 0, the injected charge from M_s/M_b is neutralized through the short circuit path, and the switch errors caused by charge injection and clock feed-through of M_s-M_b are well mitigated. Therefore, a small R_on (=50Ω) with a large switch size can be used without degrading the linearity. The harmonic distortion is also caused by ISI errors due to the rise-fall time asymmetry of the feedback RDAC. As R_on is much smaller than R_DAC (=50kΩ), the mismatch effect of R_on on the rise-fall time asymmetry is negligible. The tri-level RDAC with negative-R provides excellent alias-rejection because the impedance at the virtual ground of the 1st integrator remains constant regardless of the feedback symbol. With the tri-level RDAC and the negative-R assistance, a voltage swing at virtual ground is maintained at the level of 15mV. This, in turn, alleviates the BW requirement of the 1st opamp, which only requires the UGB of F_s to achieve HD3<-110dB. As a result, the 1st opamp consumes only 13.3μA. The negative-R is realized with cross-coupled inverters. As the operating point of negative-R is virtual ground (V_X,P, V_X,N) of the opamp, the change on its value is less than 20% over supply and temperature variations. The g_m of the negative-R is set to be 20μS to match with R_IN/R_DAC and is calibrated in the range from 15 to 28μS considering process variations on R_IN and R_DAC. The size of the negative-R is chosen to achieve the 1/f noise corner less than 100Hz.

Measurement Results
The CTDSM is fabricated in a 65nm CMOS, occupying only 0.14mm² (Fig.9). It draws only 68μW from a 1.2V supply. Fig.4 shows the measured PSD of with/without negative-R, where noise and distortion performance are greatly improved by negative-R. This work achieves the SNR/SNDR/DR of 94.8/98.2/94.1dB in a 24kHz BW. Measured SFDR is 107dB, which is achieved even without ISI tuning. The peak SNR variation of 1dB is achieved with a supply voltage from 1.1 to 1.4V (Fig.6). Fig.7 shows that the peak SNR degradations over temperature (-20 to 80°C) are less than 3dB without any calibration and this can be reduced to 1.5dB with the calibration of negative-R at room temperature. The state-of-the-art alias-rejection of -85 dB is measured at the frequency of F_s±2BW (Fig.8). Table I shows the performance summary in comparison with state-of-the-art works. This work achieves the Schreier’s FoM of 183.6/179.5/98.2dB (DR/SNDR), the highest energy-efficiency for audio ADCs published to date.

References

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Fig. 1 Proposed CTDSM architecture and its noise composition

Fig. 2 Negative-R assisted integrator: (a) Opamp noise attenuation and (b) Integrator distortion attenuation

Fig. 3 1st integrator and tri-level RDAC operation

Fig. 4 Measured PSD of w/ & w/o negative-R

Fig. 5 Measured SN(D)R versus input

Fig. 6 Measured peak SN(D)R under power supply variation

Fig. 7 Measured peak SNR under temperature variation

Table I. Performance summary and comparison

<table>
<thead>
<tr>
<th>Work</th>
<th>VLSI17 Tung</th>
<th>JSSC10 Peng</th>
<th>JSSC10 Rong</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPW (kW)</td>
<td>24</td>
<td>20</td>
<td>24</td>
<td>20</td>
</tr>
<tr>
<td>Die Area (mm²)</td>
<td>0.14</td>
<td>0.27</td>
<td>0.24</td>
<td>0.21</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>65</td>
<td>55</td>
<td>110</td>
<td>280</td>
</tr>
<tr>
<td>Peak SNDR (dB)</td>
<td>54.9</td>
<td>90.1</td>
<td>98.5</td>
<td>98.5</td>
</tr>
<tr>
<td>Peak SNDR (dB)</td>
<td>91.5</td>
<td>91.5</td>
<td>92.5</td>
<td>103.6</td>
</tr>
<tr>
<td>SNR (dB)</td>
<td>98.5</td>
<td>91.5</td>
<td>92.5</td>
<td>103.6</td>
</tr>
<tr>
<td>FoM0 (dB)</td>
<td>108.6</td>
<td>108.6</td>
<td>108.6</td>
<td>108.6</td>
</tr>
<tr>
<td>FoM0 (dB)</td>
<td>179.6</td>
<td>179.6</td>
<td>179.6</td>
<td>179.6</td>
</tr>
</tbody>
</table>

Fig. 8 Measured anti-aliasing property

Fig. 9 Chip photo