A sub-0.85V, 6.4Gbps/s/pin TX-Interleaved Transceiver with Fast Wake-up Time using 2-Step Charging Control and \( V_{OH} \) Calibration in 20nm DRAM Process

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Abstract

A sub-0.85V, 6.4Gb/s TX-interleaved transceiver with fast wake-up time using 2-step charging control and a \( V_{OH} \) calibration scheme is implemented using 20nm DRAM process. Adopting an interleaving scheme based on improved DRAM process, the proposed design operates at lowest supply voltage of 0.83V in DRAM process, and improves pin-efficiency by 30% compared with recent DRAM I/O interfaces. The fast wake-up time level shifter can achieve target switching voltage level without latency increase. And the leakage current by newly adopted transistors can be alleviated using a splitted power gating scheme.

Introduction

As the high bandwidth memory with low power consumption attracts market’s attention recently, many techniques for energy efficient high speed I/O interface have been researched. Most of these researches have relied on circuit level approaches because of the high \( V_T \) of inherent DRAM process to reduce the leakage current. However, as a transistor has its own frequency limitation, the circuit level approaches cause rapid increase in design complexity which is directly in inverse proportion to yield under low supply voltage. Thus, combining both enhanced DRAM process and the circuit level approaches which alleviate the speed limit can be an efficient solution. In this design, with fast wake-up time level shifter using 2-step charging control, a TX-interleaved transceiver in 20nm DRAM process achieves sub-0.85V 6.4Gbps/s/pin operation.

Proposed Transceiver with Fast Wake-up Scheme

As the operating speed of I/O interface in DRAM increases, signal distortion in a single data path in conventional LPDDR4X-type architecture sharply increases. Thus, valid window also rapidly shrinks in low supply voltage condition as shown in Fig. 1. Thus, an interleaving scheme and newly realizing an advanced low \( V_T \) transistor (aLVT) within the allowable leakage current in DRAM process can be efficient solutions in terms of low power signal processing with minimized hardware burden. The target propagation delay (tPD) of aLVT in this design is determined as 76% of normal LVT considering the DRAM process variations such as negative-bias temperature instability (NBTI) and leakage current (\( I_{LEAK,PMOS} \)); where \( I_{LEAK,PMOS} \) of aLVTs are increased by 4 and 3.2 times respectively compared to normal LVTs.

Fig. 2 shows a top-level block diagram of the proposed TX-interleaved transceiver with a fast wake-up time level shifter using 2-step charging control. To improve the operating speed at 0.83V supply voltage, a two-channel transmitter-interleaved architecture [1] is employed based on aLVT in 20nm DRAM. An output muxing transistor (MX) is alternately shared by two transmitters which operate at half-rate, where gate-potential is boosting by a level shifting scheme. Thus, the operating speed of the data signal which is vulnerable to ISI is alleviated to half data rate while that of clock signal which is robust to ISI is toggled at full data rate. The level shifting using 2-step charging control in the bootstrapping switch efficiently reduces the wake-up time from issuing of read command. And \( V_{OH} \) level during a periodic ZQ calibration can be adjustable by control the value of level shifting voltage (\( V_{LS} \)) using 4-bits codes. The separation of the \( V_{DDQ1} \) in main driver from the pre-driver and other circuitry makes to lower \( V_{DDQ1} \) down to 0.6V with saving in off-chip power consumption [2]. The \( I_{LEAK,LMOS/PMOS} \) caused by the aLVT is alleviated using a splitted power gating scheme using external high voltage (=1.8V). The leakage current of the main path driver can be reduced by intentionally widening the channel length having high impedance while that of the pre-driver can be reduced by a super cut-off switch.

Fig. 3 shows a specific block diagram of the proposed fast wake-up time level shifting using 2-step charging control to alleviate the slow charging time of the \( C_L \) in level shifter. Generally, in a level shifting scheme, the value of the \( C_L \) is maximized to alleviate voltage drop by capacitor dividing ratio. However, that capacitor occupies large die size and causes slow settling behavior in switching control, which causes low efficiency due to increased read latency. While increasing the weak current for fast settling in the bootstrapping switch, the current consumption during the disabled period rapidly increases. The fast wake-up time level shifter using 2-step charging control is composed of 4-sourcing / 4-sinking current sources, 2 replica level-shifting units for reference voltage generation, 2-comparators and SAR control logic. As the pre-defined reference voltages (\( V_{REFP,LS} \) and \( V_{REFN,LS} \)) are generated by replicating the weak current source without a load capacitor, fast reference voltage settling can be feasible irrespective of PVT variations. When the read command is issued, the 4-bits thermometer-weighted sourcing current sources (weight=4) start to charge the \( C_L \) sequentially in the coarse conversion period. The overshoot voltage due to quantization error is reduced by 4-bits sinking current sources (weight=1) which also are enabled sequentially during the fine conversion period. When the \( V_{LS} \) is within pre-defined target level, the settling-done flag is generated referring the outputs of the comparators and both coarse and fine current sources are automatically turned off. Thus, total settling time is reduced to below 20ns from 340ns and that reduced settling time can meet the read latency. Moreover, the valid window (VddLVW) can be guaranteed without \( V_{OH} \) drop due to the lowered \( R_{ON} \) of MX. The \( I_{W,peak} \) in the level shifter unit is divided into 7-identical current sources. And in default case, 4-identical current sources are automatically turned off.
sources are enabled and $V_{OH}$ level shift depending on the $V_T$ variation can be recovered by combination of identical current sources using MRS codes.

**Experimental Results**

A TX-interleaved transceiver with a fast wake-up time level shifter using 2-step charging control and a $V_{OH}$ control engine is implemented in 20nm DRAM process including aLVT which is targeted for high speed operation at low supply voltage condition and it occupies 0.0156mm$^2$. The proposed fast wake-up time level shifter using 2-step charging control can be verified by Shmoo results which are also correlated to S/I simulation as shown in Fig. 4. And the overall feasibility of the proposed design can be proved by using PRBS ($2^{11}-1$) patterns and measured jitter is 57ps at 6.4Gbps and 61ps at 7.4Gbps depending on the supply voltages with fixed $V_{DDQL}$ (=0.6V), respectively as shown in Fig. 5. Owing to the aLVT with the splitted power gating scheme and the TX-interleaving scheme adopting PI-LVSTL, the prototype operates at lowest supply voltage of 0.83V in DRAM process, and achieves a better pin-efficiency than previous DRAM I/O interfaces. Moreover, adopting the fast wake-up time level shifter by 2-step charging control, the TX-interleaved transmitter is feasible in DRAM normal read operation without timing loss in terms of latency. Fig. 6 shows a chip photo of the prototype design in DRAM die.

**References**

