A 0.8V 82.9μW In-ear BCI Controller System with 8.8 PEF

EEG Instrumentational Amplifier and Wireless BAN Transceiver

Jaehyuk Lee¹, Kyoung-Rog Lee¹, Unsoo Ha², Ji-Hoon Kim¹, Kwonjoon Lee¹ and Hoi-Jun Yoo¹

¹School of EE, KAIST, Yuseong-Gu, Daejeon, Republic of Korea
²MIT Media Lab, Cambridge, MA USA

E-mail: leejh612@kaist.ac.kr

Abstract

In-ear brain-computer interface (BCI) controller system is implemented with a dedicated SoC including EEG readout and body channel communication (BCC) transceiver (TRX). The 8mm² chip is fabricated using 65nm CMOS and contains 3 key features, 1) current reusing LNA (CRLNA) for low power, 2) bootstrapping DC servo loop (BDSL) enabling low noise measurement even on 350mV electrode DC offset (EDO), and 3) dual mode PGA (DMPGA) that reduces TRX power consumption by activating only when the intentional wink is present. EEG IA shows the state-of-the-art 8.8 power efficiency factor (PEF) performance, and the entire IC consumes 82.9μW. From the measurement with 9 subjects, proposed BCI system accomplished 84% average accuracy for the binary selection task.

Introduction

Recently, BCI systems based on EEG are studied as the next generation user interface (UI) technology [1, 2]. Especially, auditory steady-state response (ASSR) [2], where the EEG response to the sound stimulus shows the same frequency on the EEG spectrum as that of stimulus, can be used for the additional modality for UI. The ear EEG, compared with bulky scalp EEG of many electrodes on the head skin [2], can be measured using a robust, compact and unobtrusive means, such as the modified earphone, for monitoring the brain activity. Moreover, it can be securely worn inside of ear, semi-invasively, to avoid motion artifact [1]. Since ASSR is highly related to the temporal lobe activity, its signal-to-noise ratio measured within the ear is even higher than that of scalp EEG such as forehead. Therefore, ear EEG is good for the long-term ASSR monitoring in natural environments. However, the previous ear EEG systems were implemented with large external monitoring electronics and an earplug with electrodes contacting on the ear canal [1, 2]. Moreover, previous IC included only the EEG amplifiers without wireless communication [3]. In this work, we proposed a low power and compact in-ear BCI controller system which can operate with the small battery. Dedicated low power SoC includes power efficient EEG read-out for continuous monitoring the ASSR and employing the low power BCC TRX [4] for wireless data transmission.

Proposed In-ear BCI Controller System and SoC

Fig. 1 shows the in-ear BCI controller system and its operation. In the BCI module, the proposed SoC powered by a zinc-air battery (100mAh, <0.3g) is integrated. BCI operations and communication is activated by intentional wink which is separable to spontaneous blinks [5]. By initialization with the intentional wink, external sound signals start stimulating the right ear at 43Hz and the left ear at 37Hz. After short time delay, either 43Hz or 37Hz frequency component of Ear-EEG signal itself goes up selectively as the user pays attention to either his right ear or left ear, respectively. Fig. 2 shows the overall block diagram of the proposed SoC. It consists of 2-Ch EEG IA, 11'b SAR ADC, digital controller, and BCC TRX [4]. The EEG IA includes three key features: CRLNA, BDSL, and DMPGA

A. CRLNA and BDSL Circuit

Fig. 3 shows the schematics of CRLNA. In order to maximize power efficiency, CRLNA operates with a 0.8V supply. To achieve high open loop gain (>100dB) requirements of EEG IA, two-stage topology including OTA1 and OTA2 is employed. OTA1 has the doubled-gm by adopting the current-reusing folded-cascode topology [6], however, additional current source (M6) is newly included for common mode feedback of CRLNA. Therefore, the proposed OTA1 structure combines not only the doubled-gm of the inverter-based OTA but also large open loop gain (>75dB) of the folded-cascode OTA. Fig. 4 shows the schematic diagram of BDSL. EEG IA employs the chopping technique for enhancing the CMRR and noise characteristics. Chopped amplifier requires a DSL to avoid the LNA saturation by EDO. The BDSL uses a coarse digital DSL and a fine analog DNL to decrease overall LNA noise [7], but it reduces the LNA noise further by cutting CDSL by half through bootstrapping clock generator. A 50pF is included to boost up to 2VDD clock to reduce the size of CDSL by half for the same EDO rejection. At 350mV EDO condition, the noise amplification factor is 14.2% lower than that of [7]. Fig. 5 shows the transfer function and noise spectrum measurement results of CRLNA and BDSL. CRLNA achieves a 40dB gain, 95dB CMRR. BDSL generates 0.5Hz HPF corner, and measured 0.32μVrms, 0.38μVrms noise in the presence of 20mV, 350mV EDO.

B. Dual Mode PGA (DMPGA) Circuit

Fig. 6 shows the DMPGA circuits and its measured transfer function. Since the intentional wink is responsible for BCI activation in standby mode, an accurate and power efficient wink detection is required. DMPGA supports dual mode by adding switches to the feedback path. In EEG mode, PGA operates as an amplifier because its gate is biased by just the off-current leakage of the switch. In Wink mode, CDS periodically samples the current voltage input. Only the voltage difference between sampled voltages at t-1 and t is amplified by the PGA to detect the transition edges without ECG artifacts. The LPF corner is adjusted by anti-aliasing filter (AAF) for the attenuation of power line artifacts. The DMPGA generates ~10 times higher output voltage for intentional wink than spontaneous blinks. Wink detector unit wakes up BCC TRX within 0.5s after the wink is detected. In standby time, only CRLNA and DMPGA are activated consuming low power of 5.7μW, and in active mode the proposed SoC consumes 82.9μW for full BCI operation.

Implementation Results and Conclusions

Fig. 7 shows the system measurement results. In ASSR measurement, the user hears the modulated sound signals with 43Hz at right ear and 37Hz at left ear simultaneously. If user’s attention is not enough, the corresponding EEG peak frequency slightly deviates from the stimulus frequency, and both the amount of amplitude increase and the frequency deviation are used as the features for classification. The classification accuracy increases to 66, 80, and 84% as the length of the time slot is to 5, 10, and 15 seconds. As shown in Fig. 7, the combinations of attention directions can be used as the command signals to control the music player on smart device.

Fig. 8 shows the chip micrograph and performance summary. BCI controller SoC is fabricated in 65nm CMOS process. It
occupies 8mm² and dissipates 82.9μW when the 2-Ch EEG IAs and BCC TRX are activated. Thanks to the CRLNA and BDSL, the proposed SoC can measure EEG with state-of-the-art 8.8 PEF even on 350mV EDO condition of dry electrodes. ASSR is clearly measured with spectrogram at 37Hz and 43Hz frequencies for left and right attention, respectively. The proposed compact, low power and robust ear-EEG system enables the smart mobile BCI devices by using the combinations of ASSR signals as the control signals.

References

Fig. 1 In-Ear BCI System
Fig. 2 Overall Block Diagram
Fig. 3 Current Reusing LNA (CRLNA)
Fig. 4 Bootstrapping DC Servo Loop (BDSL)

Fig. 5 Measured Waveform of CRLNA and BDSL
Fig. 6 Dual Mode PGA (DMPGA)
Fig. 7 Measured ASSR and BCI Classification Results
Fig. 8 Chip Micrograph and Summary

TABLE I. EEG IA PERFORMANCE COMPARISON TABLE

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