A 64μs Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier

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Abstract

This paper presents a low-energy and quick start-up 26/40 MHz crystal oscillator for IoT wireless communications. The negative resistance is boosted to reduce the start-up time by using a reconfigurable multi-stage amplifier during the start-up period. A variable feedforward path implemented in the multi-stage amplifier can overcome a conventional limitation of the negative resistance. At 40 MHz oscillation, the proposed crystal oscillator fabricated in 65 nm CMOS demonstrates a start-up energy and time of 37.2 nJ and 64 μs, respectively.

Introduction

Wireless sensor nodes in IoT applications have to operate with duty-cycling to reduce power consumption. A crystal oscillator (XO), which is used to generate a stable reference clock for transceivers and microcontroller units, also requires duty-cycle operation. Generally, start-up time ($T_s$) of XO is relatively long (~ms) due to the high-quality factor of crystal resonator. The long $T_s$ causes higher start-up energy ($E_s$) especially for highly duty-cycled transceiver with a short packet format. Therefore, $T_s$ should be minimized by using a reduction technique with low overhead in power consumption. Fig.1 shows a conventional crystal oscillator, the start-up time $T_s$, and negative resistance $|R_n|$ characteristics with respect to its circuit parameters [1]. To reduce $T_s$ and $E_s$, prior-arts report several techniques [2-4]. According to equation of $T_s$ in Fig.1, there are three techniques, such as increasing $|R_n|$ [2, 4], increasing $|I_{d}(0)|$ [2, 3], and decreasing $C_t$ [4]. A conventional negative resistance boosting (NRB) technique [2] can increase $|R_n|$, however, it cannot reduce $E_s$ because $|R_n|$ is proportional to a trans-conductance $g_m$ of an amplifier. Moreover, $|R_n|$ is limited due to the parasitic capacitance of crystal resonator $C_t$. This paper presents a low power NRB technique by using a reconfigurable multi-stage amplifier. Furthermore, a feedforward path is embedded in multi-stage amplifier to break through the conventional limitation on the value of $|R_n|$.

Multi-stage amplifier with feedforward path

Fig.2 shows a conceptual diagram of the proposed multi-stage amplifier. The concept is very simple, two stage amplifiers are implemented in front of a trans-conductance stage such as Fig. 2 (a). The effective trans-conductance $g_{m,\text{eff}}$ can be boosted to $A_1 A_2 g_m\alpha$. The power efficiency of the proposed NRB is improved because the required trans-conductance of $g_{m1}$ and $g_{m2}$ is much smaller than $g_{m,\text{eff}}$. In the case of a simulation condition in Fig.2, the effective trans-conductance is boosted to 100x with a power overhead of only 1.67x. However, the limitation of $|R_n|$ is still an issue. To break the limitation, a feedforward path is implemented in a multi-stage amplifier as shown in Fig. 2 (b). This feedforward path realizes a "zero" in the frequency response and drastically improves $|R_n|$ around the oscillation frequency. Fig.2 (c) shows the frequency response of $|R_n|$ in each amplifier. The simple multi-stage amplifier improves $|R_n|$ at 40MHz from 42 Ω to 524 Ω compared to the conventional single stage amplifier. Furthermore, by implementing the feedforward path, $|R_n|$ is improved to 5900 Ω, which is $7\times$ higher than the limitation value of the single amplifier.

Circuit Implementation

Fig. 3 shows a top level schematic of the proposed multi-stage amplifier. It consists of three stage amplifiers and a 4-bit variable capacitor, which is used to form the feedforward path. Each amplifier stage consists of a resistive feedback inverter circuit with enable terminals. The 1st and 3rd stage amplifier are used as boost amplifiers, and 2nd stage amplifier is used as both boost and steady state amplifier. The boost amplifier has two switches S1 and S2 for switching between operating as a resistive feedback amplifier and passing through a signal. Fig. 4 shows a timing diagram of the proposed amplifier. During the boost period, all amplifiers are enabled (XO_EN=High, BST_EN=High), S1 in boost amplifiers turns on to form the resistive feedback inverter. In the steady state (XO_EN=High BST_EN=Low), boost amplifiers are disabled and S2 turns on to short the input and the output of the boost amplifiers, thus only the 2nd stage is enabled to keep the oscillation. During power off period, all amplifiers are disabled. The 4-bit variable capacitor is used to control the frequency response of $|R_n|$ to keep the desired peak point against to circuit parameter changes and PVT variation. A unit capacitance of $C_u$ is 100 fF, so variable range is 1.5 pF.

Measurement Results

The chip was fabricated using 65 nm LP CMOS and the occupied area is only 0.0053 mm², as shown in Fig. 8. Fig. 5 shows the measured start-up time vs. amplifier configurations at both oscillation frequency of 26 MHz and 40 MHz. The variable capacitor code is set to 0111 for 26 MHz and 0000 for 40 MHz. The boost ON time also affects the start-up time, so we set it to 50 μs in the typical condition. The measured start-up behavior with and without NRB at oscillation frequency of 40 MHz is shown in Fig. 6. The start-up time is defined as the duration for the frequency to settle to within ±40ppm away from the target frequency. Without NRB, XO takes 1150 μs to start-up. In contrast, with NRB, the frequency can settle in 64 μs, resulting 18x in $T_s$ reduction. Fig. 7 shows the measured start-up time with respect to temperature and voltage variations. $T_s$ is relatively stable for temperature variation (±10%) and supply variation (61%). Table 1 and Fig.9 summarizes the performance of proposed XO. The proposed XO demonstrates the fastest start-up time with the highest $T_s$ reduction ratio. The start-up energy is also effectively reduced by using the proposed NRB. Furthermore, core area is much smaller than the other works due to the simple architecture.

Acknowledgement

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References

Fig. 1 Conventional crystal oscillator and negative resistance.

Fig. 2 Conceptual diagram of a multi-stage amplifier.

Fig. 3 Top level schematic of the proposed multi-stage amplifier.

Fig. 4 Timing diagram of the proposed crystal oscillator.

Fig. 5 Measured start-up time vs. amplifier configurations.

Fig. 6 Measured start-up behavior with and without NRB.

Fig. 7 Measured start-up time stability over wide temperature and voltage range.

Fig. 8 Chip photo. CI/CI:Chirp/Dither Injection, DAL:Dynamically Adjusted Load

Fig. 9 Measured $T_s$ and $E_s$ reduction ratio comparison.

TABLE I Performance Summary

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>This work</th>
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<tr>
<td>Core area (μm²)</td>
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<td>Supply voltage (V)</td>
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<td>Frequency (MHz)</td>
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<tr>
<td>Gain stage</td>
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<td>6</td>
<td>12</td>
<td>9</td>
</tr>
</tbody>
</table>

Start-up time ($T_s$) (μs) | 158 | 435 | 200 | 76 |
Start-up time ($E_s$) (μs) | 40  | 45  | 46  | 40 |
Gain stage reduction ratio | 13.3  | 8.2  | 13.3 | 30 |
Temperature range (°C) | -30~+125 | -30~+125 | -30~+125 | -30~+125 |
Power OFF | 10000 | 10000 | 10000 | 10000 |

$E_s$ is estimated with the start-up power of 2x the steady-state power.