New methodology for evaluating minority carrier lifetime for process assessment

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Abstract

A new methodology to evaluate the process temperature dependence of the minority carrier lifetime has been developed. A TEG layout with p'-stripes on an n-Si substrate was designed. When all the p' n junctions are made forward, the minority carrier diffusion current flows one dimensionally into the substrate. On the other hand, for making only the one center p' n junction forward, the current spreads laterally and flows cylindrically into the substrate. By the difference in the flow path of the minority carrier diffusion, we can successfully extract the minority carrier lifetime. We applied the methodology to the evaluation of the minority carrier lifetime depending on the process temperatures and confirmed the lifetime degradation for high temperature process.

Introduction

Evaluation of minority carrier lifetime is important for designing the switching performance of pn-based devices [1] as well as the sensitivity of image sensors and photovoltaic devices. Minority carrier lifetime is strongly influenced by the quality of wafers (defects, O and C atoms), and by processes, especially by thermal treatments [2] (fig. 1). A rough estimation of the lifetime is performed by photo-conductance measurements on separately prepared bulk wafers with mimic thermal processes [3]. However, it is difficult to evaluate the lifetime electrically on devices. For example, hole lifetime (τp) evaluation in n-base or n-drift layer in IGBT has been a fitting parameter in device simulators to reproduce the measured I-V curves or transient behaviors. One-dimensional diode measurements can directly extract the τp [4], yet the accuracy will be lost when the target τp is long (fig. 2) [5]. pn diodes combined with photoexcitation measurements allow us to extract τp over the wide range, but cannot be integrated into test-element groups (TEGs) [6]. Therefore, the purpose of the study is to propose a methodology to extract the τp over the wide range by electrical measurements.

TEG Design for Carrier Lifetime Extraction

By forming a stripe p' region on an n-base layer, the excess holes diffuse and disperse into the n-base layer, maintaining the wide-base conditions (fig. 3). Hole concentration profile reveals a steep drop near the injected region even with long τp (fig. 4). The TEG design consists of 5-stripe pn diodes in parallel with a pitch of Wp, which enables the measurement of the center diode under forward-bias condition, that is applying a negative voltage to the common cathode (Vc). When the rest of the anodes are open, current spreading into the n-base occurs depending on the τp and injection level of holes (“Single setup”). With all anodes grounded (“Multi setup”), holes are confined in the slab with a width of Wp (fig. 5). The difference in the voltage drop (∆V) of the n-base region under “Single” and “Multi” conditions reflects the magnitude of current spreading, which is a good indicator for τp. The relationship between τp and Wp is discussed through device simulations.

Device Simulation

Device simulations were conducted on p'n diodes under different hole lifetimes (from 0.3 μs to 300 μs) and an n-base thickness of 725 μm. ∆V shows a linear relationship with log(Wp) under low current density (J) of 106–107 A/cm2 with τp=300μs (fig. 6), thus the intercept to the x-axis (Wp,max) can be determined. At τp=3μs, the slope deviates with wider Wp due to the contribution of the spreading resistance (Rp) of the n-base region (fig. 7). Therefore, the slope in the narrow Wp region should be used to determine the Wp,max. A plateau in Wp,max in low J region strongly reflects the τp (fig. 8). Indeed, log(τp) and log(Wp,max) show a linear relationship over τp≥10μs, and can be approximated by Wp,max=1.34Lp, where Lp is the diffusion length of holes (fig. 9).

Demonstration of Process Assessment

The proposed TEGs were fabricated on an n-type FZ-Si(100) with an N0 of 2×1016 cm−3 and a thickness of 380 μm. The initial τp of the wafer measured by μ-PCD was 156 μs. Diode fabrication process is shown in fig. 10. To evaluate the influence of thermal processes to τp, thermal oxidation (for T=33nm) at either 1050°C or 1100°C for 13 min or 5 min, respectively, was performed. ∆V on Wp for the control diode without additional thermal process shows the same behavior as the simulation ones (fig. 11). Extrapolated Wp,max also shows plateaus at low J region (fig. 12). The extracted τp for the control, 1050°C-oxidized and 1100°C-oxidized diodes are 61 μs, 33 μs and 18 μs, respectively (fig. 13). Summing the reciprocals, we can extract the process limiting lifetime (τp,add) for each process. A large degradation was confirmed with high temperature oxidation, supported by [7]. This result is consistent with the concept of scaling IGBTs with advantage of long τp [8].

Conclusions

A methodology to extract τp over the wide range that can be integrated into Si wafers was proposed. Diode pitch dependent voltage drop, the difference between “single” and “multi” setups, produces an indicator Wp,max, which can be expressed with the τp. Process assessments were demonstrated at different oxidation temperatures. It was confirmed that high temperature oxidation degrades the τp strongly.

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**Fig. 1** (a) Cross-section of a typical IGBT. \( \tau_p \) in n-base region influences the IGBT performance. The proposed TEG for \( \tau_p \) estimation in this study.

The proposed TEG for \( \tau_p \) extraction is shown in (b). The process compatibility with device fabrication and direct on-wafer \( \tau_p \) extraction are also demonstrated.

**Fig. 2** \( J_0 \) for different \( \tau_p \) with different n-base thickness. \( J-V \) of 1D diode loose sensitivity for target \( \tau_p \).

**Fig. 3** pn diodes with a stripe layout geometrically preserves wide-base conditions.

**Fig. 4** Excess hole distribution in a cylindrical coordinate system can be analytically expressed. A steep drop near the junction results in maintaining the wide-based conditions for cylindrical diodes.

**Fig. 5** (a) “Single” and (b) “Multi” setups for \( I-V \) curve measurements of the center diode. The current spreading can be probed by changing the \( W_p \). \( \Delta V \) is the difference of the potential drop in the base region. Contact resistance \( r \) can be cancel out.

**Fig. 6** \( \Delta V \) on \( W_p \) at different \( \tau_p \) with \( \tau_p = 30\mu \text{s} \). A same \( W_{p\text{max}} \) was obtained from \( 10^7 \) to \( 10^8 \) A/cm².

**Fig. 7** \( \Delta V \) on \( W_p \) at different \( \tau_p \) with \( \tau_p = 3\mu \text{s} \). Spreading resistance \( R_s \) of the base region becomes dominant at large \( W_p \).

**Fig. 8** \( W_{p\text{max}} \) on \( \tau_p \) with different \( \tau_p \). A constant value can be extracted at low injection.

**Fig. 9** \( W_{p\text{max}} \) on \( \tau_p \). \( \tau_p \) can be extracted with high sensitivity over \( \tau_p = 10\mu \text{s} \). \( W_{p\text{max}} = 1.34L_p \) is a good approximation.

**Fig. 10** Diode fabrication process flow. A target process was performed prior to the diode fabrication. In this study, oxidation temperature for \( T_{ox} = 33 \text{nm} \) was evaluated.

**Fig. 11** Measured \( \Delta V \) and \( W_p \). \( W_{p\text{max}} \) can be obtained by extrapolation. An identical \( W_{p\text{max}} \) was obtained from \( J \) of \( 10^5 \) to \( 10^4 \) A/cm².

**Fig. 12** Each \( W_{p\text{max}} \) on \( \tau_p \) clearly shows a plateau. The effect of oxidation process to \( \tau_p \) is evident.

**Fig. 13** A \( \tau_p \) over 10 \( \mu \text{s} \) can be easily extracted. With this analysis, low temperature oxidation is effective to preserve the \( \tau_p \).

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**References**