High-speed Voltage Control Spintronics Memory (VoCSM) 
Having Broad Design Windows

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Abstract
Voltage Control Spintronics Memory (VoCSM) is a magnetic memory combining the spin Hall effect and Voltage Controlled Magnetic Anisotropy (VCMA). It has the potential to make MRAM work faster. In this paper, we described memory design of a write window and a read window of high-speed VoCSM from experimental data. The design windows of both writing and reading are large enough for gigabit memory.

Introduction
Energy saving of working memories is attracting great interest because of the recent rapid increase in energy consumption due to the information explosion on the internet. Non-volatile working memory has a possibility of saving energy. Among many non-volatile memories MRAM is the most promising candidate for non-volatile working memory because of its fast write speed and potentially long life-time. Spin-Transfer-Torque (STT) writing is energetically efficient technology for MRAM and extensively investigated. However, as STT requires write and read currents to pass through a tunnel barrier as shown in Fig. 1(a), its memory design window would be limited because of breakdown voltage and read disturbance. Voltage-control spintronics memory (VoCSM) a new architecture combining the spin Hall effect and Voltage Controlled Magnetic Anisotropy (VCMA), has been proposed to overcome this technical challenge [1-5]. The write current and the read current flow in different paths as shown in Fig. 1(b). The concept of the VoCSM has been already proved [1-5]. In this paper, we discuss the memory design windows for writing and reading of the high-speed VoCSM with experimental data.

Memory concept of High Speed VoCSM
The high-speed VoCSM is designed for cache memory. A diagram of its memory cell is shown in Fig. 2 [2-3]. Two MTJs are aligned on an electrode that has high spin Hall efficiency. Write current flows in the electrode in an opposite direction for these two MTJs through a VIA located between them. Therefore, when one MTJ is in a parallel (P) state, the other is in an anti-parallel state. This enables read time to be faster with a differential read amplifier. Voltage is applied to the MTJs while writing in order to reduce the write current by the VCMA that is shown in Fig. 3. As shown in Fig. 4, nanosecond order pulse switching is available by increasing the write current.

Experiments
The Fabricated layer stack structure of the MTJ for VoCSM was IrMn(8nm)/CoFe(1.8nm)/Ru(0.8nm)/CoFeB(1.2nm)/MgO(1.6nm)/CoFeB(1.2nm~1.6nm)/Ta based bottom electrode (8~10nm)/substrate. The spin Hall efficiency of storage layer CoFeB(1.2nm~1.6nm) is θSH=0.18 and VCMA efficiency is about 80 fJ/Vm. The size of the MTJ was 30nm~60nm and the aspect ratio was 2.5~3.0. The process detail is described elsewhere [4]. A STEM image of the MTJ is shown in Fig. 5.

Memory design window for writing
One of the merits of the VoCSM is a broad writing window. In VoCSM, the writing-path is not the thin tunnel barrier but the bottom electrode with high melting temperature. Fig. 6(a) shows switching currents of MTJs by 20ns pulse as an inverse function of MTJ resistance that is proportional to MTJ area. It shows that the switching current strongly depends on the size of MTJ which can be improved by lithography. Therefore we estimate the remaining switching current variation by excluding the MTJ area variation as shown in Fig. 6(b). The remaining 1-sigma value of the switching current is estimated to be around 10%.

The switching current density as a function of pulse width of various MTJs is shown in Fig. 7. The switching current density of 5 ns pulse is about 10MA/cm² and is 50% larger than that of 20ns pulse.

The breakdown current density of the VoCSM was estimated by measuring the resistance change of the bottom electrode when the accelerated write pulse voltages are applied to the bottom electrode of 60 nm width and 3um long without the MTJ. The pulse width was 20 ns and the current density was 80MA/cm² which was the largest current density for our apparatus. The result is shown in Fig. 8. Although this is an accelerated test in the current density and the electrode size, the resistance was not changed that means electromigration does not degrade the electrode. A memory design window for writing of the high-speed VoCSM is shown in Fig. 9(a). The switching current density, its sigma value and the breakdown current density are derived from Fig. 7, Fig. 6 and Fig. 8, respectively. Real breakdown current density is larger than that shown in Fig. 9(a) because no degradation was measured on 100 times longer electrode than a real memory. Its sigma value is set to 7%. We can set the write current density to be 30MA/cm² with a sigma of 5% without overlap between the switching current and the write current. There is no overlap between the write current and the breakdown either which means that the write window is large enough for gigabit memory.

On the contrary, as shown in Fig. 9(b), the write window of the STT MRAM has the overlap between the write current and the breakdown. The switching voltage is set to 0.4V [6] and the breakdown is set to 1.8V. Same sigma value was used as Fig. 9(a).

Memory design window for reading
One of the merits of the VoCSM is a broad reading window. In VoCSM, the polarity of read voltage is chosen to enhance the switching energy. If resistance area product (RA) is set large, there is no read disturbance at all. If the RA is relatively small and the read voltage is set extremely large, appreciable read current flows to apply STT to disturb. Therefore, we measured STT switching rate of the MTJ for the VoCSM whose RA is 100 Ωμm² resulting in no switching detected by 2×10⁸ pulses of 1.6 V on the MTJ. Therefore, we measured STT switching of the MTJ whose RA is 10 Ωμm² instead and converted the result by shifting the voltage. The result is shown by a broken line in Fig. 10. The measurement result of the 100 Ωμm² MTJ indicates that its STT disturbing rate is lower than 1×10⁻⁷, shown by the blank circle, even with extremely large voltage of 2 V in Fig. 10 which is consistent with our estimation. It is concluded that there is no read disturbance with the actual reading voltage of 0.4V.

Fig. 11 describes MTJ resistance as a function of DC...
voltage applied on the MTJ showing that breakdown voltage of the tunnel barrier is about 2.1V.

Fig. 12(a) describes a memory design window for reading of the high-speed VoCSM. The read voltage is set to 0.4V and its sigma value is 5%. The STT switching rate and MTJ breakdown voltage are estimated from Fig. 10 and Fig. 11, respectively. Their sigma values are set to be 10% and 7%, respectively. The same sigma value 10% as the spin Hall switching is used for STT. There is such a broad window between the read voltage and STT switching meaning that no read disturbance occurs on the VoCSM. It is quite a contrast to the STT MRAM as shown in Fig. 12(b). The read voltage and switching current overlap even the read voltage is reduced to 0.2V and the same sigma value is used.

**Conclusion**

The design windows for writing and reading of the high-speed VoCSM were estimated from the experimental data. A sufficient window for gigabit memory was proved.

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**References**