A 0.3pJ/bit 112Gb/s PAM4 1+0.5D TX-DFE Precoder and 8-tap FFE in 14nm CMOS

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Abstract

We present a digital implementation of a TX precoder/equalizer that, similar to a Tomlinson-Harashima Precoder (THP), provides a decision feedback equalizer (DFE) function on the transmitter side. The TX-DFE avoids error propagation together with the complexity and power overhead of an RX-DFE. The 1-tap precoder is implemented using a table-based digital FFE, which also shapes the channel pulse to a 1+0.5D response and cancels pre-cursor inter-symbol interference (ISI). The combined precoder/8-tap FFE was implemented in 14nm FinFet CMOS, and was measured to operate at 112Gb/s consuming 0.3pJ/bit energy.

Introduction

To satisfy the increasing bandwidth demand in computer systems and networks, electrical links are rapidly moving to data rates above 100Gb/s using PAM-4 signaling. At channel attenuations above 20dB, PAM-4 requires precise equalization and a DFE to achieve low bit error rates. At these high data rates, however, it is hard to implement DFEs at the RX side due to the short feedback loop.

As an alternative, the DFE can also be implemented at the TX side, which is usually referred to as Tomlinson-Harashima Precoding (THP)[1]. Implementing a THP was so far considered prohibitive at high-speed operation due to its high complexity and short loop-delay requirements. However, the implementation can be simplified by shaping the channel into a 1+0.5D response, which is close to the natural channel response for ~20dB loss channels. Fig. 1A displays an example implementation of a classical single-tap THP for a 1+0.5D channel: The ISI of the channel is cancelled by feeding back the output of the summation node after a modulo operation. A successive FFE cancels the pre-cursor ISI, and shapes the channel into a 1+0.5D response. There are two issues with this implementation: First, it is hard to close the feedback-loop timing including the modulo operation, and second, the FFE is power hungry since it needs to work on 6-8bit quantized values.

These deficiencies can be overcome with the proposed solution shown in Fig. 1B: Here, the symbols are first fed into a remapping stage, which remaps PAM-4 symbols in order to be received correctly without RX feedback operation. Then this stream of remapped PAM-4 symbols is supplied to a table-based FFE, capable of combining two distinct pulse responses, one for symbols +/-1, the other for symbols +/-3.

Pre-Coder Functionality

A. Basic Idea

The basic idea for the pre-coder is seen in Fig 2: Given that the transmitted PAM-4 signal levels are {-3, -1, +1, +3}, without pre-coding there are 10 distinct levels after the 1+0.5D channel at the RX: {−4.5, −3.5, −2.5, −1.5, −0.5, 0.5, 1.5, 2.5, 3.5, 4.5}. It can be easily seen that it is possible to convert these 10 distinct levels to only 5 levels {−4, −2, 0, +2, +4} by adding or subtracting a small correction value \( \delta = +/-0.5 \).

The sign of this \( \delta \) correction value depends on the previous symbol: If the previous symbol was in {-3, +1} or {-1, +3} the sign is positive or negative, respectively. This results in a 5-level pre-coded signal constellation (denoted PPAM-5 in Fig. 2), where the upper and lower levels both correspond to the 2-bit PAM value “00” = -3.

B. Symbol remapping

As indicated by the colored dots in Fig. 2, the following recursive symbol remapping is applied in case the previously remapped symbol \( y_{n-1} \) was in \{+1, +3\}:

\[
 y_n = \begin{cases} 
 x_n & \text{if } y_{n-1} \in (-1, -3), \\
 x_{n,\text{mod}} & \text{if } y_{n-1} \in (+1, +3),
\end{cases}
\]

with \( x_{n,\text{mod}} = +3, -3, -1, +1 \) for \( x_n = -3, -1, +1, +3 \), respectively, and \( x_n \) and \( y_n \) denoting the input and output PAM-4 symbols of the remapping stage.

C. ISI cancellation for \( \delta \) correction pulses

Since the channel is 1+0.5D, it is necessary to cancel the ISI of the \( \delta \) pulse by applying the inverse of the channel to it:

\[
 \delta' = \frac{\delta}{1+0.5z} = \delta - \frac{\delta}{2}z^{-1} + \frac{\delta}{4}z^{-2} - \frac{\delta}{8}z^{-3} + \ldots
\]

Although this in theory would require an IIR filter, in practice the response can be cut and approximated with a 5 tap...
FIR filter with negligible error. Fig. 3 displays the resulting pulse responses including the $\delta$ corrections for symbols +3 and +1. (The pulses for the negative symbols -3 and -1 are just the inverted versions.) The actual filter coefficients for the FFE are derived by convolving the two pulse responses with the FFE shaping response $h(n)$:

$$f_3(n) = g_3(n) * h(n),$$

$$f_1(n) = g_1(n) * h(n).$$

(3)

Comparison to standard FFE case

Given a 1+0.5D channel, it is easy to show that cancellation of the post-cursor with an FFE under maximum amplitude constraint results in an attenuation of the cursor by 2. The proposed precoder attenuates the cursor by 4/3 since it needs additional signal overhead to accommodate the $\delta$ corrections (which is the same value as in a standard THP for PAM-4). Comparing the two, precoding results in a 3/2 higher cursor value than the standard FFE, which corresponds to 3.5dB gain. It is straightforward to extend the proposed precoding circuit to $\alpha > 0.5$ (which needs a 6-level constellation instead of the 5-level constellation for $\alpha=0.5$). Fig. 4 displays the amplitude gain of the cursor over FFE as a function of $\alpha$.

Fig. 4. Precoder gain over FFE for 1+$\alpha$D channel.

Advantage of TX-DFE precoding vs. DFE

A TX-DFE avoids error propagation. This makes it possible to apply FEC only on the LSBs, which enables a reduction of the coding overhead by 2 by using set partitioning as shown in Fig. 5. Secondly, the RX for the proposed PPAM-5 signals only require 4 comparators to slice the data. Thirdly, a 1-tap TX-DFE enables building a multi-tap RX-DFE for taps 2-n: Since tap 1 is cancelled by the TX, a RX-DFE for taps 2,3..n can be easily implemented since the feedback timing is now at least 2UIs. (Note that the DFE coefficients $h_2..h_n$ need to be convolved with $1/(1+0.5z)$ response.) Another advantage is that the dynamic range is reduced to +/-4 from +/-4.5 in the DFE case, relaxing the linearity requirements.

Digital Implementation

The symbol remapping stage (Fig. 6), which implements the recursion (1), uses a 5-level deep MUX tree structure with speculation to meet timing.

The implementation of the table-based FFE is shown in Fig. 7. There are 4 distinct tables, each corresponding to 2 FFE taps. Each table contains all 16 combinations of +/-f1 and +/-f3. Using symmetry only the first 8 entries need to be stored, and the symmetrical values can be derived by inverting the outputs using one-complement inversion.

The four values from the table are added together and rounded by cutting the 2 LSBs. The resulting 8-bit output then goes into an 8-bit 56GS/s DAC [2].

Measured Results

The precoder/FFE was synthesized in 14nm FinFet CMOS into a 150x150µm² digital logic block using standard library cells, and then combined with the DAC on a 1x0.5mm² test chip (Fig. 8). Fig.9 displays the correct 112Gb/s PPAM-5 data eye using the precoder/FFE with a 7.25inch 21dB loss channel, together with the equalized PAM-4 eye. At 112Gb/s the pre-coder/FFE operates at 1.75GHz consuming 33.7mW at 0.7V digital supply, which corresponds to 0.3pJ/bit (including also a PRBS pattern generator). The power overhead of the precoder/FFE over a standard 8-tap FFE is negligible. The overall TX including the DAC consumes 2.4pJ/bit.

Fig. 8. Test chip layout including Precoder/FFE and DAC [2].

Fig. 9. Measured equalized PPAM-5 and PAM-4 eyes.

References