A 112Gb/s PAM4 Wireline Receiver using a 64-way Time-Interleaved SAR ADC in 16nm FinFET

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Abstract— A 112Gb/s PAM4 wireline receiver testchip is implemented in 16nm FinFET. The receiver consists of continuous-time linear equalizers, a peaking capacitance buffer, and a 56Gs/s 64-way time-interleaved SAR ADC. The receiver achieves 2e-5 BER over a 20dB loss channel at 28GHz Nyquist while consuming 590mW power, excluding DSP.

112Gb/s electrical interface represents a significant increase in the data rate over existing 56Gb/s solutions. While enabling support for top-of-rack to middle-of-rack over copper it also facilitates electrical optical interface efficiency beyond 100Gbps where multiple links would traditionally be required. PAM4 is the adopted signaling method and is therefore compatible with existing 56Gbps standards. This limits the frequency content of the signal to 28GHz and below. An ADC [1][2] based receiver design is chosen so that recovered data can be further equalized using Digital Signal Processing (DSP) techniques to correct for channel impairments. PAM4 signaling at 56Gb/s and beyond requires FEC. At 112G, the pre-FEC raw BER of <1e-4 is a typical target [3].

Figure 1 shows the receiver block diagram. The analog front-end provides signal equalization and conditioning, reducing the resolution and full-scale-range requirements of the ADC [4]. The differential analog input is converted into 7-bit digital values by the 56Gs/a/s ADC. An on-chip DSP consisting of a 31-tap FFE and 1-tap DFE equalizes the recovered symbols from the ADC and supplies these to the on-chip CDR and PRBS error checker. The pre-DSP ADC outputs are periodically stored in an on-chip 64Kb storage and read into an off-chip FPGA that performs equalization adaptations and ADC offset/gain/skew calibrations.

The Analog Front End (Figure 1) comprises 3 stages of equalization and an AGC. The first and second CTLE stages are designed to provide programmable levels of high frequency peaking to compensate for signal loss near Nyquist with a constant DC-gain of around 0dB. The third CTLE stage compensates for mid-frequency losses (long tail equalization) [5] while the AGC has a 10dB programmable DC gain range to optimally scale the signal to the full scale input range of the ADC.

The receiver employs a 7-bit, 56Gs/a/s 64-way time-interleaved SAR ADC (Figure 2). The ADC supports an input range of 600mV diff-pp. Two stages of cascaded 8-way time-interleaving are used. In Rank-1 stage the input is sampled and held using eight-phase, non-overlapping 7GHz clocks. In the Rank-2 stage each of the Rank-1 output signals are further sampled and held using a set of 8-phase 875MHz clocks. These sampled values are converted using 8 instances of a SAR ADC clocked at 875MHz. The 64 converted output codes are re-timed to a single 875MHz clock domain and provided to the on-chip DSP.

The timing skew calibration of the eight-phase 7GHz clocks and the gain/offset calibration of the 875MHz ADC instances are performed using pseudo-random data input. This removes the needs for foreground calibration and reduces the dependency on complicated system sequencing. The timing skew calibration is performed in the analog domain and the gain/offset calibration is done in the digital domain.

The bandwidth requirement for the Rank-1 switches results in them having a large input capacitance and requires significant signal path buffering, provided by the Rank-1 NMOS source followers (Rank-1 SF). This represents a significant load on the AGC stage of the CTLE. In order to obtain the required bandwidth of the AGC an additional stage of buffering was added to isolate the Rank-1 SF load from the CTLE (referred to as the Pre-ADC Buffer in the Figure 1).

In order to mitigate against any linearity concerns introduced by this buffer a peaked source follower topology (Figure 3) was chosen rather than a CML type buffer. This buffer uses series...
inductive peaking to compensate for bandwidth losses in the source followers. The design provides for a programmable amount of peaking. The design and layout was carefully tuned to trade off peaking and avoid group delay distortion. Constant gm biasing was used to keep the both the bandwidth and the peaking of these stages constant over process, voltage and temperature.

The receiver uses a Phase Interpolator (PI) based clock and data recovery (CDR). The analog CML PI mixes differential CML quadrature clocks to generate a clock that has a controlled phase offset from the input clocks. This allows the correct alignment of the sampling position to the center of the data eye. The PI mixes the 14GHz quadrature input clocks from the PLL to generate a differential output signal at 14GHz.

In order to generate the eight 7GHz sampling phases the design utilizes two PI blocks in parallel with control codes offset. This generates 4 phases which are offset by 45°. A further divide by 2 is required to obtain the 8 phases at 7GHz. The two dividers are synchronized at reset time to ensure correct phase alignment at their outputs.

The linearity of the PI (output delay versus input code) is very important as any non-linearity will produce a code dependent skew offset between the two groups of the generated 8-phase clocks. This will be particularly of concern in a system which has ppm offset between transmitter and receiver as the Rank-1 skew correction algorithm will not have the tracking bandwidth to track any offset.

One 112Gb/s RX lane with clock distribution (PLL not shown), and DSP block is fabricated in 16nm FinFET (Figure 5).

The link performance is tested by connecting a Keysight M8057A pattern generator to the receiver over a channel with 20dB loss at 28GHz (Figure 6a). The pattern generator is configured to send 400mV diff-pair 112Gb/s PAM4 PRBS-31 signal with ~2dB pre-tap and ~1dB post-tap equalization. The on-chip PRBS-31 checker reports 2e-5 BER. Figure 6b and 6c show the post-DSP eye diagrams and sample values of the four PAM4 levels (sampled at the CDR lock point) over 8K symbols.

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 16nm FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply ((V_{\text{avcc}}, V_{\text{vtt}}, V_{\text{aux}}))</td>
<td>0.9V, 1.2V, 1.8V</td>
</tr>
<tr>
<td>Receiver Active Area (excluding DSP)</td>
<td>0.674mm²</td>
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<tr>
<td>ADC Power (including ADC clocks)</td>
<td>475mW</td>
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<tr>
<td>BER at 112Gb/s (PRBS-31)</td>
<td>2x10⁻⁵</td>
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<tr>
<td>Receiver Power at 112Gb/s (Does not include DSP)</td>
<td>590mW</td>
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<tr>
<td>PLL and Clock Distribution Power at 112Gb/s</td>
<td>165mW</td>
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</tbody>
</table>

Table 1. Performance Summary

Acknowledgments

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References