A 112-Gb/s PAM4 Transmitter in 16nm FinFET
KeeHian Tan1, Ping-Chuan Chiang1, Yipeng Wang1, Haibing Zhao1, Arianne Roldan2, Hongyuan Zhao1, Nakul Narang1, Siok Wei Lim1, Declan Carey3, Sai Lalith Chaitanya Ambatipudi2, Parag Upadhyaya2, Yohan Frans2 and Ken Chang2
1 Xilinx, Singapore  2 Xilinx, San Jose, CA, USA  3 Xilinx, Cork, Ireland

Abstract
This work reports a 112-Gb/s low power voltage-mode transmitter (TX) with four-tap feed forward equalization (FFE), designed and fabricated in 16nm FinFET technology. The design includes a hybrid impedance controller with dual regulator architecture for independent swing, common-mode and equalization control. The 56-Gb/s 4:1 multiplexer (MUX) array together with an automatic phase alignment technique is proposed to minimize output jitter. The TX consumes 345 mW and provides 0.6 to 1-Vpp output swing. The PAM4 TX achieves 130-fs random jitter (RJ) with ratio of level mismatch (RLM) > 0.963.

I. INTRODUCTION
For next generation 400-Gb/s or 1-Tb/s data transmission, a transceiver running beyond 100 Gb/s is needed. For example, as suggested by 400G-LR4, a 4×100-Gb/s scheme with wave division multiplexing (WDM) in optical domain is proposed [2]. In this paper, we present a fully-integrated transmitter with high resolution FFE taps which has up to 2% of supply voltage tuning step for TX adaption. In the proposed TX, all data-path blocks are realized in digital circuits to achieve low power consumption and high noise margin.

II. TRANSMITTER ARCHITECTURE
The transmitter is depicted in Fig. 1. It consists of a 128:4 serializer, a 4:1 multiplexer (MUX) array, a MSB/LSB driver array, a 28-GHz PLL, a duty cycle corrector (DCC) and an automatic clock phase aligner to optimize the clock phase in the last MUX stage. The serializer combines the incoming data into 4×14-Gb/s bit stream, and the FIR machine determines the 4-tap magnitudes based on different channel settings. A replica MUX is used and its output,\(D_{\text{out,rep}}\), served as the feedback signal which brings the timing information to the calibration logic. Due to the large bandwidth required, a T-coil network is designed at the TX output to isolate the 120-fF ESD parasitics. The source-series terminated (SST) driver includes a hybrid impedance controller with dual regulator DACs. Both the duty cycle and IQ mismatch are detected by low-pass filters in three low pass filters (LPF), a finite state machine and two 8-bit PAM4 operation.

\[\text{mW of power at 56 Gb/s.} \]

It is worth noting that \(C_{K0}\) and \(C_{K100}\) needs to be aligned with the internal 28Gb/s data streams, \(D_1\) and \(D_2\), otherwise the \(D_{\text{out}}\) bit width will be distorted and hence the output jitter will be increased due to this misalignment.

In order to overcome PVT variation, a background clock calibration is designed in this work. As shown in Fig. 3, there are three steps for the DCC and phase aligner: (1) Calibrate I-Clock (\(C_{K0,180}\) duty cycle), (2) Calibrate Q-Clock (\(C_{K0,270}\) duty cycle and (3) Calibrate IQ mismatch. For step 1 and 2, the duty cycle of complementary clocks is adjusted by delaying their rising or falling edges. After calibrating the duty cycle to 50%, the loop determines whether I- or Q-Clock should be delayed then shifts its rising and falling edges by the same amount.

The replica MUX provides timing information of internal 28-Gb/s DCC logic.VCDL1 TO VCDL2:

\[
\begin{align*}
\text{Fig. 2. 56Gb/s 4:1 multiplexer.} \\
\text{Fig. 3. Duty cycle correction steps.}
\end{align*}
\]

The DCC and phase aligner are depicted in Fig. 4(a). Here, the IQ mismatch is defined as the timing deviation of \(C_{K0}\) and \(C_{K100}\) from the data bit center of \(D_1\) and \(D_2\) [Fig. 2(a)]. The two voltage-controlled delay lines (VCDL) correct the clock duty cycle and IQ mismatch. Figure 4(b) illustrates the DCC logic, which consists of three low pass filters (LPF), a finite state machine and two 8-bit DACs. Both the duty cycle and IQ mismatch are detected by low-pass filtering the clock waveforms. Afterward, the calibration FSM will sense and correct the duty cycle until the differential output from LPF are equal.
Gb/s data, $D_1$ and $D_2$. As shown in Fig. 5, by connecting $D_{in,t}$ to [0,1,0,1], we can generate 14-GHz clock at nodes $D_1$ and $D_2$, also a 28-GHz clock will be obtained at $D_{out,rep}$. Since $D_1$ and $D_2$ inside the replica MUX has edge transitions at the same time as those 28-Gb/s data in the main MUX, the phase alignment is accomplished by minimizing the differential low passed $D_{out,rep}$. Note that if the skew between $CK_0$ and $D_{out,rep}$ in Fig. 5 is larger than $\pi$ ($TCK/2$), the polarity at the comparator input (inside the FSM) will be flipped and hence the calibration will diverge. To solve this issue, the replica MUX input must be adjustable to either [0,1,0,1] or [1,0,1,0] by $V_{cal,dir}$ and hence make sure the calibration always move toward the direction of convergence.

### III. EXPERIMENTAL RESULTS

The transmitter was fabricated in 16nm FinFET. It consumes 345 mW of power at 112 Gb/s, from 0.9-V, 1.2-V and 1.8-V supplies. Figure 7 depicts (a) the phase noise plot and (b) clock pattern output jitter of the 28-GHz built-in PLL. It shows an integrated rms jitter (from 3-MHz to 14-GHz offset) of 85 fs, and $-109$-dBc/Hz phase noise at 1-MHz offset. The real-time scope measures 130-fs, rms random jitter (RJ), 210-fs,pp periodic jitter (PJ), and 150-fs,pp duty cycle distortion (DCD) with 56-Gs/s clock pattern.

The PAM4 TX waveform with PRBS7 is shown in Fig. 8(a). It is measured with package, 3-inches of Megtron 6 PCB trace, and 24-inch coaxial cable into Keysight DSA96204Q oscilloscope. The channel loss without the coaxial cable is 7 dB at 28 Gb/s. However, due to the impedance discontinuity from the package BGA ball, as indicated by the pulse response from Fig. 8(b), besides 4-tap FFE from the transmitter, the FFE equalization function from the oscilloscope is activated to provide the waveform at 112 Gb/s. Figure 9 reveals the die photographs and performance summary.