Fully integrated OOK-powered pad-less deep sub-wavelength-sized 5-GHz RFID with on-chip antenna using adiabatic logic in 0.18 μm CMOS

Yuta Toeda, Takumi Fujimaki, Mototsugu Hamada, Tadahiro Kuroda
Keio University, Yokohama, Kanagawa, Japan

Abstract
A fully integrated pad-less 5-GHz RFID was developed in a 0.18 μm standard CMOS. It integrates an on-chip antenna, an RF-to-envelope power converter, a 128-bit ROM, and a load modulation circuit. It occupies 2.1 mm X 1.2 mm, and is much smaller than the wavelength of the carrier frequency. The ROM is implemented by an adiabatic shift register driven by a power clock, generated by the RF-to-envelope power converter. It is capable of 10 kBps backscattering communication at a distance of 10 cm with 24 dBm EIRP.

Introduction
The main metrics of an RFID are its cost, form factor, and range. An external antenna to increase the communication range also increases the cost and form factor; therefore, integrating an antenna on a chip without increasing the other two metrics is desirable. In this regard, the miniaturization of antennas was insufficient compared to the wavelength in [1]. In [2], the communication range is too short although the size is very small. In this paper, we propose a new system architecture to solve these problems.

System Architecture
A. Overview
Fig. 1 shows a block diagram and operation waveforms of the developed RFID, compared with those of a conventional one. The developed RFID consists of an on-chip antenna, an RF-to-envelope power converter, a 128-bit adiabatic ring shift register, and a load modulator. For the developed RFID, duty-cycled RF power, i.e. on-off keying (OOK) power, is fed instead of constant envelope power as used in existing RFID systems. The output of the RF-to-envelope power converter is a duty-cycled voltage source, i.e. a power clock. The power clock drives an adiabatic ring shift register, which is programmed through the wiring of its dual-rail signals, making it possible to store a unique ID by customizing only one mask layer. The output of the shift register is connected to the load modulator for backscattering communication that reflects its unique ID. By using adiabatic logic with OOK power, we can reduce the average feeding power. Compared to existing RFID systems, the required received power can be reduced by a factor of 1/4 when using adiabatic logic and OOK power, which has a duty ratio and modulation rate of 10% and 10 kbps, respectively. The combination of simple power conversion to the power clock and adiabatic or non-constant-voltage sourced logic operation enable the proposed system’s small size and power efficiency.

B. Adiabatic ring shift register
Fig. 2 shows the operation of the adiabatic ring shift register. For simplicity, the figure depicts a 4-bit case; however, it can be expanded to larger shift registers. A single register consists of an NMOS adiabatic shift register (NASR) [3] and a PMOS adiabatic shift register (PASR). By combining PASR and NASR (PNASR), the shift register can be driven by a single-phase power clock because PASR operates at the rising edge of the power clock and NASR at the falling edge.

In this work, the output of a 128-bit shift register is connected to its input to form a ring shift register. The ring shift register generates a unique bit sequence depending on the connections between registers. For example, in the 4-bit case shown in Fig. 2, there are four connections between registers. Each connection can be either “straight,” i.e. a non-inverting connection, or “cross,” i.e. an inverting connection. Supposing that all four OUTP are “1” and all four OUTN are “0” at the first rising edge of the power clock, the output bit sequence at OUT is 10011001…10011001, which reflects “cross,” “straight,” “cross,” “straight” connections. By changing the polarity of the connections, we have 16 patterns of bit sequences in the 4-bit case, which can be extended to 2^n patterns in the n-bit case. The very limited customization will be done by an electron beam lithography on a chip-by-chip basis.

We will now explain how to set up the initial state in which all four OUTP are “1” and all four OUTN are “0” at the first rising edge of the power clock, as shown in the right half of Fig. 2. For this purpose, we have an offset at the input stage of PASR. Transistors with a larger gate width are employed in Mp3 and Mp4 compared with Mp1 and Mp2. A charge path through Mp3 and Mp4 is stronger than that through Mp1 and Mp2.

C. Developed RFID
Fig. 3 shows the details of the developed RFID including the circuit diagrams of the RF-to-envelope power converter and the load modulator [4] with full-chip simulation results. The RF-to-envelope power converter is a 6-stage CMOS cross-coupled charge pump with a resistive load so that it outputs the envelope of OOK power. When the antenna input level is –20 dBm, the power clock is a pulse train with a peak height of 1.8 V. The shift register generates ID, 1001 in this case. Depending on the value of the ID, the load is modulated, which can be seen as the difference of the re-radiated power that has a peak height ratio of about 2:1.

D. On-chip antenna
Fig. 4 shows the design and characteristics of the on-chip antenna. It is a double-loop antenna with output impedance designed to be conjugate-matched with the RF-to-envelope power converter. The double loop structure contributes to the miniaturization of the antenna. Its gain is ~26 dBi, and its size is 2.1 mm X 1.2 mm, which is 0.037 λ X 0.021 λ at 5.25 GHz.

Experimental Results
The chip micrograph is shown in Fig. 5. Fig. 6 gives the measurement setup and results of backscattering communication using the developed RFID chip. The OOK power is sent to the RFID chip from a distance of 10 cm with 24 dBm EIRP. The chip shows its own ID, which is monitored by an oscilloscope. The chip has an output buffer driven by a separated power source for this purpose. The re-radiated power, in addition to the stray radiation of the incident power, is monitored by a different antenna at a distance of 10 cm. A power detector connected to the antenna outputs Rx signal, which matches the unique ID of the RFID chip.

The performance summary of the developed RFID chip, compared with those of [1] and [2], is shown in Table 1. We compared the results using two types of FOM. FOM1 is intuitively understood as an inverse of the square root of the power received by an antenna. The better the FOM1, the less power the RFID consumes. This work has the highest FOM 1 and is 102 times better than [2], which employs a similar backscattering system. In
FOM2, the square root of the area is normalized by the wavelength because the miniaturization of the antenna can be evaluated using its size relative to the wavelength. Our system exhibited a FOM 2 that was 13.5 times better than [1]. These results demonstrate that a mm-sized RFID operating at a 5-GHz band is possible. Its compactness has the potential to enable new applications of RFID systems such as chip-scale implantation in the human body and technology for traceability.

References


Fig. 1 Block diagram of standard and proposed RFID system.

Fig. 2 Proposed adiabatic ring shift register.

Fig. 3 Proposed RFID system with circuit diagrams and full-chip simulation results.

Fig. 4 Design and characteristics of on-chip antenna.

Fig. 5 Chip micrograph of developed RFID chip.

Fig. 6 Measurement setup and results of backscattering communication.

Table 1 Performance summary with benchmark results.