Half-and-Half Compare Content Addressable Memory with Charge-Sharing based Selective Match-Line Precharge Scheme

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Abstract
In this paper, we present a half-and-half compare contents addressable memory (HHC-CAM) to reduce the dynamic power consumption as well as white space between the cell array and peripheral. In the proposed HHC-CAM, by splitting the match-line (ML), almost 99% of entries are filtered out in first half-side comparison. Thanks to the reduced ML switching capacitance, 42% lower energy delay product (EDP) is achieved compared to the conventional selective precharge approach. The proposed 16KB, 10T-NOR CAM macro, has been fabricated in a 14nm FinFET technology, and the chip measurement results show the energy consumption of 0.38fJ/search/bit (560ps search delay), which is the best EDP reported in literature.

Introduction
As a high-speed search engine, CAM has been widely used in network routers and many associative computing applications. One of the main advantages of the CAM is to support parallel comparison (Fig. 1) for high-speed search operation, which incurs very large dynamic power consumption. To reduce the power, selective precharge is frequently used as an ML sensing [1-5]. However, the selective precharge needs divided bitcell array, thus increasing the white space between the cell array and peripheral. Especially, in FinFET technology, the white space between two blocks that have different fin pitches, becomes even larger compared to planar device. In this paper, we propose an HH-CAM that significantly improves EDP while pushing the bitcell array rolled into one.

Proposed Half-and-Half Compare CAM
Fig. 1 shows the conventional CAM architecture and two popular CAM cell topologies. Generally, NOR-type CAMs are preferred to NAND-type CAM [1] due to threshold voltage (VTH) loss across ML. The proposed CAM cells are based on the basic NOR-type cell structure. As shown in Fig. 1, the main difference between the proposed NOR-type CAM cells and the conventional ones are 1) separated ML (shown in the right part of Fig. 1), and 2) parallel BL and ML, which are proposed to provide low-power and high-density features. The proposed transposed cell configuration facilitates SRAM-like binary CAM (BCAM) layout by placing the source/drain of ML column-wise. Since the most of lookup table has static data, the proposed transposed cell configuration which induces the column-wise entries, can be easily implemented. The proposed BCAM cell based HHC-CAM array has been designed as shown in Fig. 2. For the search-line (SL) drivers, two enable signals (SLE and SLBE) are used to separately access both-side of the bit-compare circuit in a CAM cell. For each entry which is laid on column-way, the charge-sharing based selective precharge (CSSP) scheme is employed to reduce the ML power consumption. The overall operation of the proposed HHC-CAM operation can be summarized as follows. To initialize the CAM data, the transpose of the static lookup table data is written to CAM cells (CAM entries are stored in column-way). Prior to the CAM search operation, the half-side MLs (MLSLb), which are connected to the first half-compare circuit, are precharged to VDD while the other half-side MLs (MLSLa) and one-side BLs are precharged to VSS. After that, the SLBE signal is activated to filter out the mismatched entries for the first half-side comparisons. During this pre-search operation, the precharged-high MLs are selectively discharged to VSS for the S0D1 case, which means that the search data (S) is ‘0’ and the stored data (D) is ‘1’. As shown in the timing diagram of Fig. 2, the post-search result (MLD) is used to correct final output. For the survived entries during the pre-search, the other half-side comparisons (post-search) are performed using the charge-sharing manner. As shown in Fig. 2, the remaining charge on the matched MLs (in the pre-search phase) is reused for the precharged-low ML (MLSL). When the two ML node voltages have the equal value (VTH), the SLE signal is fired to compare the other half-side. At this time, the precharged-low BL and the charge-shared ML that were used in pre-search phase, are exploited to generate the reference voltage (VREF). In this second charge-sharing, the VREF is formed between VEQ and VSS. Compared to the previous ML sensing schemes [1-5], which require additional capacitors (dummy cells or physical capacitors) and external tuning, the proposed approach easily facilitates differential ML sensing at the cost of negligible area overhead (< 2%).

Detailed Comparisons with Previous Works
Detailed comparisons between the conventional selective precharge ML sensing [1-5] and the proposed HHC scheme is presented in Fig. 3. As shown in the N x M CAM array, the conventional selective precharge initially searches only the first k-bits and then searches the remaining N-k bits for the matched entries. As shown in Fig. 3 and Fig. 4 (top-left), since the conventional approach uses locally partitioned array, the area cost caused by the white space between the cell array and peripheral can be doubled. On the other hand, the proposed HHC-CAM can make the bitcell array rolled into one. The switching capacitances incurring the major dynamic power and switching delay are summarized in the top-right table of Fig. 3. During two search phases, the total switching capacitance for the SLs in both approaches are equal to N x CSL. The separated ML of the proposed HHC-CAM is reduced to half of ML switching capacitance per an entry. Although the selective precharge allows smaller ML switching capacitance than the proposed HHC-CAM in the first search-phase, the large ML switching capacitance of the second search-phase induces significant performance degradation. As shown in Fig. 4 (top-right), in the worst-case condition (1b-mismatch), the selective precharge shows extremely wide distribution (×1.0 to ×10.7 for mean value) of ML discharging delay. On the other hand, in case of the proposed HHC-CAM, thanks to the separated ML, the narrow distributions (×1.7 to ×2.9) of ML discharge delay are observed.

In order to examine the skipping rate for the second search-phase, a 3-bit search example is illustrated in Fig. 3. As shown in Fig. 2 and Fig. 3 (bottom-left), the 50D1 cases can be considered as a mismatch case in the pre-search phase of HH-CAM. Since the same number of ‘0’ induces identical mismatch probability (e.g. 001, 010, and 100 have 6/8 mismatch probability), the mismatch probability can be represented as the bottom-right table of Fig. 3. In case of selective precharge, 1/2 entries are survived in the second search-phase. The numerical results are presented in Fig. 4 (bottom-left). When the width of pre-search data is over 16, ~99% of the search operation in both of two approaches can be skipped in second search phase. The EDP comparison is shown in Fig. 4 (bottom-right). Compared to the baseline (all precharge) and selective precharge based CAM, the proposed HHC-CAM shows 42% and 19% of EDP savings, respectively, with the nominal supply voltage of 0.8V.

Measurement Results
Fig. 5 shows a die micrograph of a 14nm FinFET 16KB CAM test-chip. It is designed with two 128×64 CAM macros, 1.8V GPIO, and 84nm gate-pitched standard-cell logics. The die-area of the test
chip is 4.8 mm². Measurement results and comparison table are presented in Fig. 5 and Fig. 6, respectively. As shown in the shmoo plot, the 300mV and 380mV of minimum operation voltages are obtained for VSD and VSL, respectively. Compared to the state-of-the-art [5], the proposed HHC-CAM achieves 22.5% improved search speed at the cost of 18% FOM (U/bit/search) increase.

References

Fig. 1. The conventional CAM array architecture, and the proposed NOR-type CAM cells.

Fig. 2. Array structure with the proposed 10T-NOR BCAM cell and related timing diagram.

Fig. 3. Comparison between the conventional selective pre-charge and the proposed half-and-half compare scheme.

Fig. 4. Simulation results.

Fig. 5. Measured results.

Fig. 6. Comparison table.